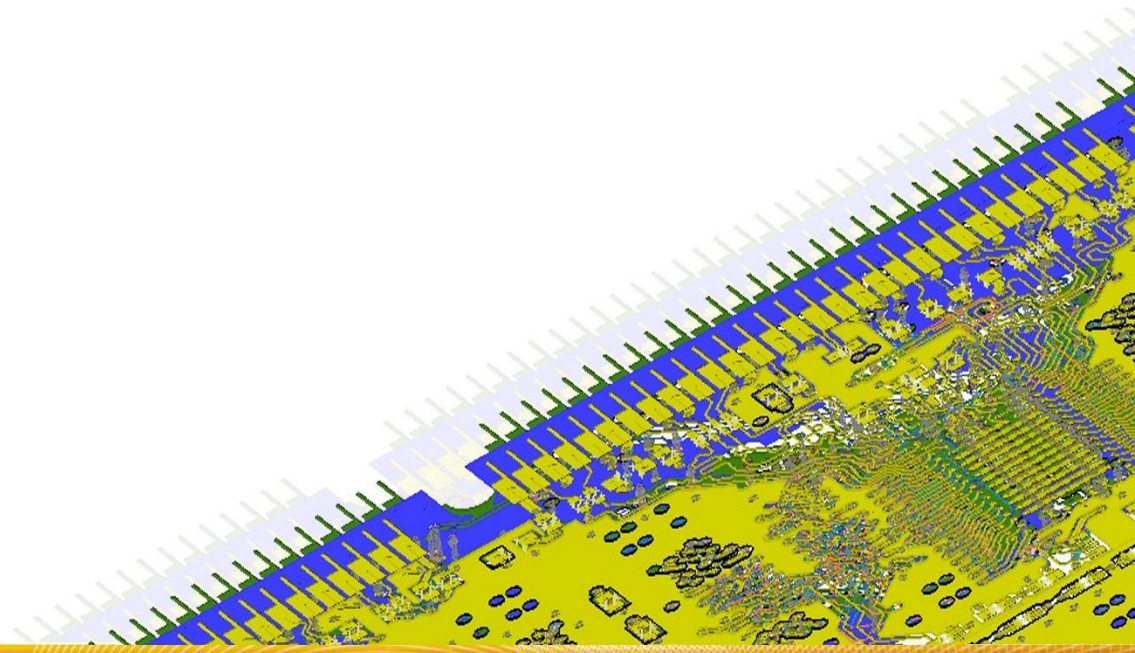
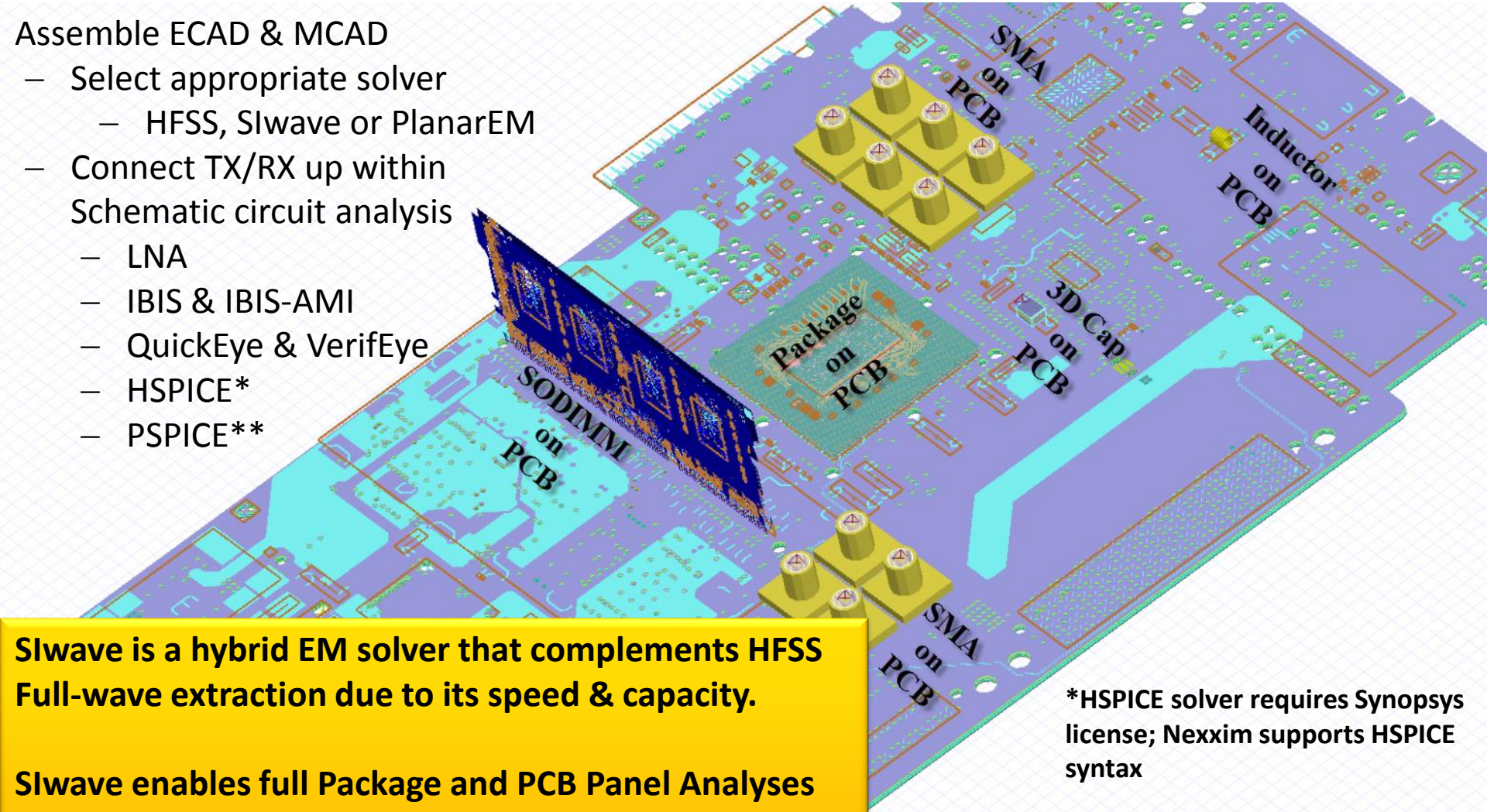
ANSYS®

What is SIwave?



Virtual System Analysis with HFSS & SIwave

Assemble ECAD & MCAD
- Select appropriate solver
  - HFSS, SIwave or PlanarEM
- Connect TX/RX up within Schematic circuit analysis
  - LNA
  - IBIS & IBIS-AMI
  - QuickEye & VerifEye
  - HSPICE*
  - PSPICE**



SIwave is a hybrid EM solver that complements HFSS Full-wave extraction due to its speed & capacity.

SIwave enables full Package and PCB Panel Analyses with a high fidelity hybrid solver.

SIwave includes Nexxim PI/SI/EMI circuit capabilities to provide end-to-end solutions/work flows.

***HSPICE solver requires Synopsys license; Nexxim supports HSPICE syntax**

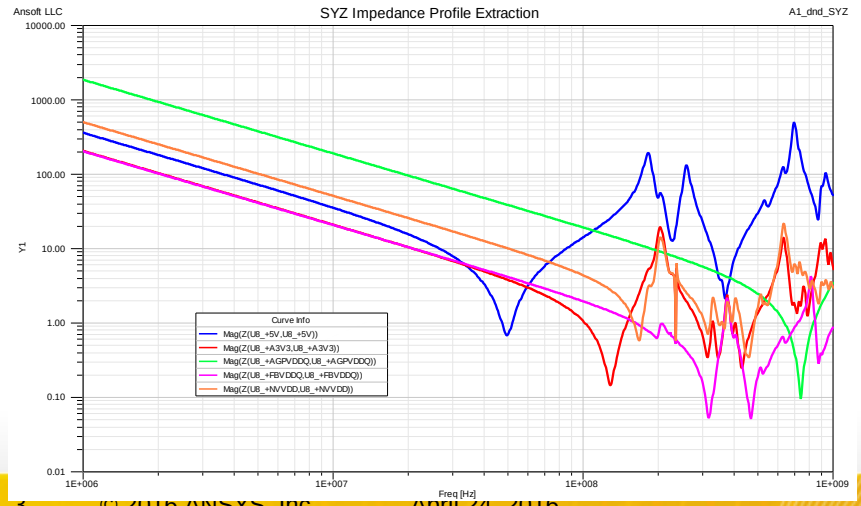
**** Uses Nexxim solver with PSPICE syntax**

ANSYS

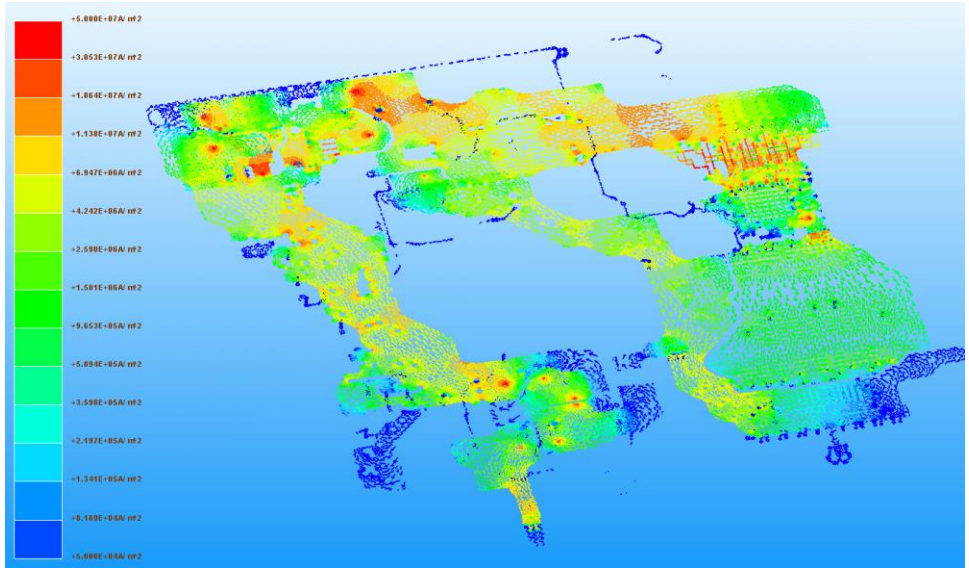
SIwave

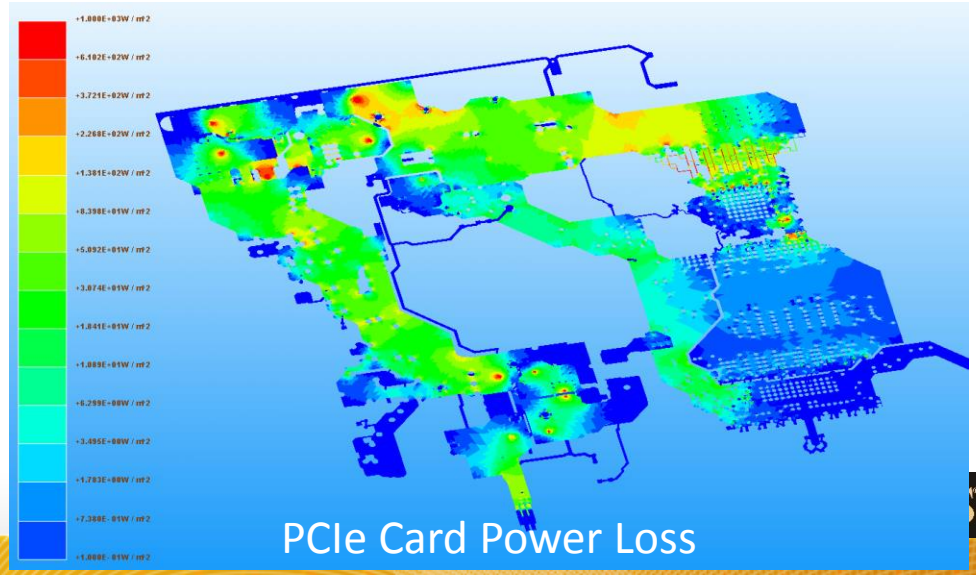
What is SIwave?

- Hybrid 2.5D full wave EM field solver
- Models layered structures
- Analysis performed
  - Signal Integrity
  - Power Integrity
  - DC IR drop analysis
  - EMI/EMC
  - Decoupling capacitor optimization
  - PSPICE, HSPICE, & Spectre ckt analysis



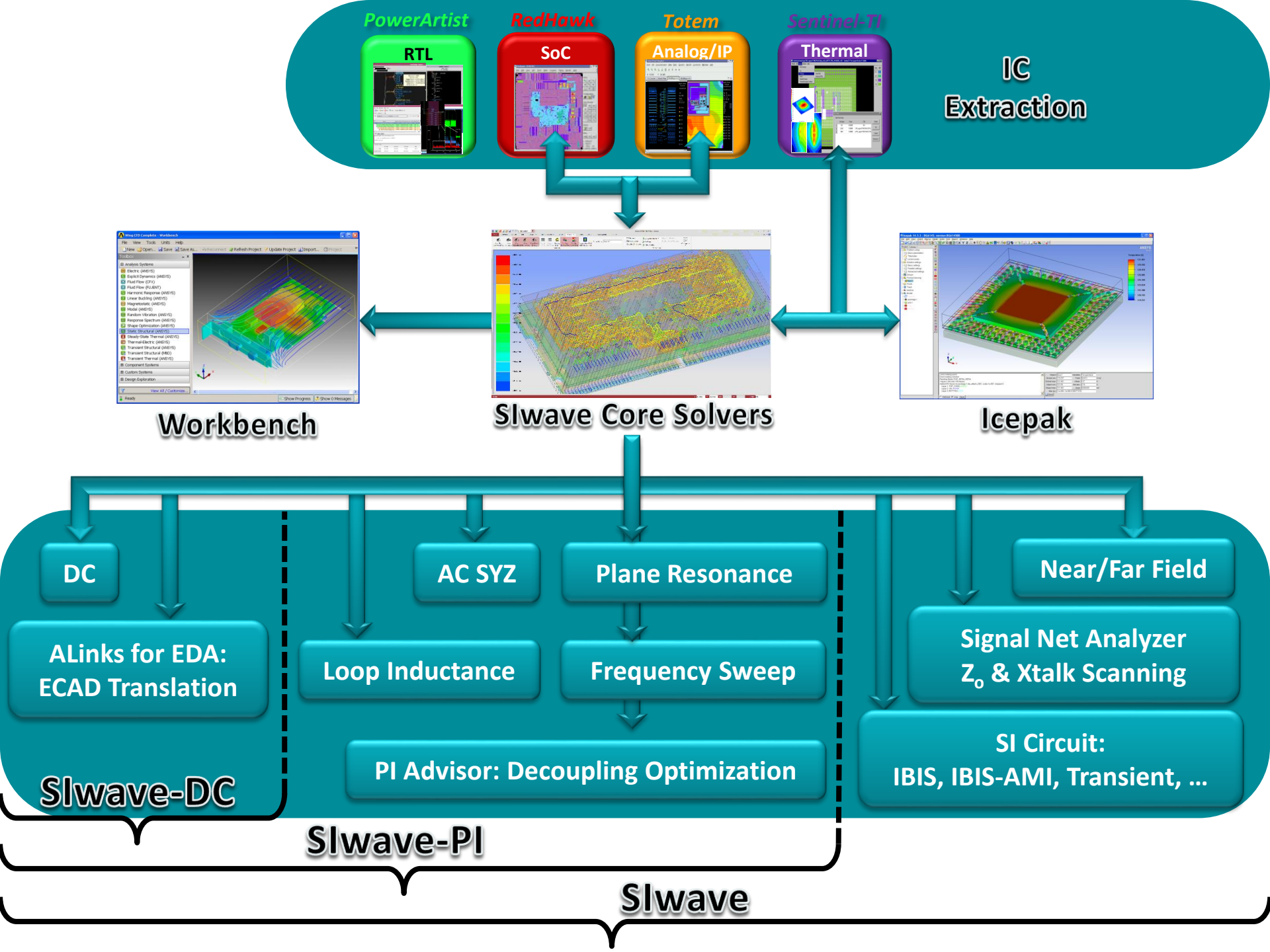
PCIe Card Power Distribution





Supported ECAD Translations

- **Cadence**
  - Allegro ⇒ 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6
  - APD ⇒ 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6
  - SiP Digital/RF ⇒ 16.0, 16.1, 16.2, 16.3, 16.5, & 16.6
  - Virtuoso ⇒ 5.10, 6.14, 6.15, & 6.16 (Linux only)
- **Mentor Graphics**
  - Expedition ⇒ v2005, v2007.1 thru EE7.9 (uses HKP design flow)
  - Boardstation ⇒ 8.x (uses HKP design flow)
  - Boardstation XE ⇒ v2007, v2007.1, v2007.2, v2007.3 and v2007.7 (uses HKP design flow)
  - PADS ⇒ PowerPCB v5.2a, v2005 and v2007 (ASCII Flow)
- **Zuken (Sold by Zuken)**
  - CR5000 ⇒ 10 and higher (Zuken translator for .anf & .cmp)
  - CR8000 ⇒ 2013 and higher (Zuken translator for .anf & .cmp)
- **ODB++**
  - Altium Designer ⇒ R10 and greater
  - Mentor Expedition ⇒ EE7.9.1 and greater
  - Mentor PADS ⇒ 9.4 and greater
  - Zuken Cadstar ⇒ 12.1 and greater
- **IPC-2581**
  - Pulsonix ⇒ Revision 8.5 build 5905 and greater
- **Other ECAD Formats**
  - .anf ⇒ ANSYS neutral file format
  - .gds ⇒ IC Chip format
  - .xfl ⇒ Apache Sentinel format
  - .dxf ⇒ AutoCad drawing format
    - Added Lead Frame Editor capability to SIwave and ANSYS Electronics Desktop


PowerArtist
RTL
RedHawk
SoC
Totem
Analog/IP
Sentinel-TI
Thermal
IC Extraction
Workbench
SIwave Core Solvers
Icepak
DC
ALinks for EDA: ECAD Translation
AC SYZ
Loop Inductance
Plane Resonance
Frequency Sweep
PI Advisor: Decoupling Optimization
Near/Far Field
Signal Net Analyzer Z_o & Xtalk Scanning
SI Circuit: IBIS, IBIS-AMI, Transient, …
SIwave-DC
SIwave-PI
SIwave

Functionality	SIwave – DC	SIwave – PI	SIwave
ECAD Translation	✓	✓	✓
SIwave & 3D Layout GUI	✓	✓	✓
I^2R DC solver (Joule Heating with Icepak)	✓	✓	✓
DC Path Resistance Solver	✓	✓	✓
Plane Resonance Solver		✓	✓
Automated Decoupling Analysis Optimization		✓	✓
AC SYZ Solver		✓	✓
AC Frequency Sweep Solver		✓	✓
Synopsys HSPICE Integration		✓	✓
Z_o Scanner (Single Ended & Differential)			✓
Cross-talk Scanner			✓
TDR Wizard			✓
Near-Field EMI solver			✓
Far-Field EMI Solver			✓
Flight Time Signal Net Analyzer			✓
Circuit Analysis (IBIS, IBIS-AMI, .tran, .ac, …)			✓
Network Data Explorer & Macro-modeling			✓
Conducted & Radiated EMI with Circuits			✓

SIwave – DC

- **A product offering specialized for predicting DC power delivery issues within PKGs and PCBs.**

1. **The solver uses a unique *Adaptive Mesh Refinement* process to ensure highly accurate predictive analyses for *Chip, Packages, and Printed Circuit Boards* which include ECAD primitives such as planes, traces, vias, bondwires, solderballs and solderbumps.**

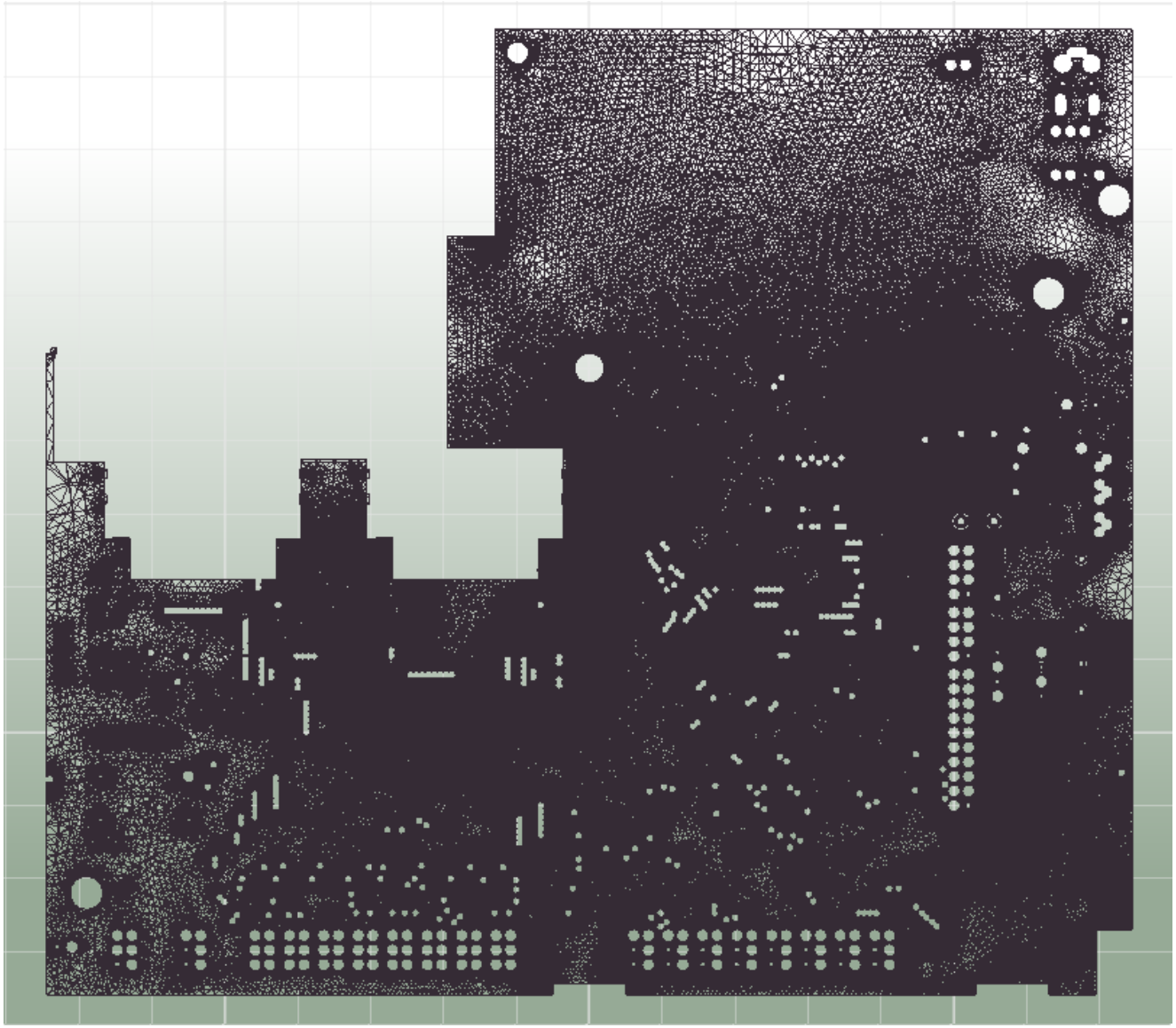
2. **Produces the following analytic results**
   - **DC voltage drop (Voltage) for all nets including GND and V_{dd}**
   - **DC current direction (Amps/Area^2) that includes return paths**
   - **DC current magnitude (Amps) into and out of vias**
   - **Power density (W/Area^2) and power loss (Watts) per layer**

3. **Has bi-directional coupling to Icepak to account for thermal losses (joule heating)**

4. **Automated reports for user defined pass/fail criteria using .html formats**

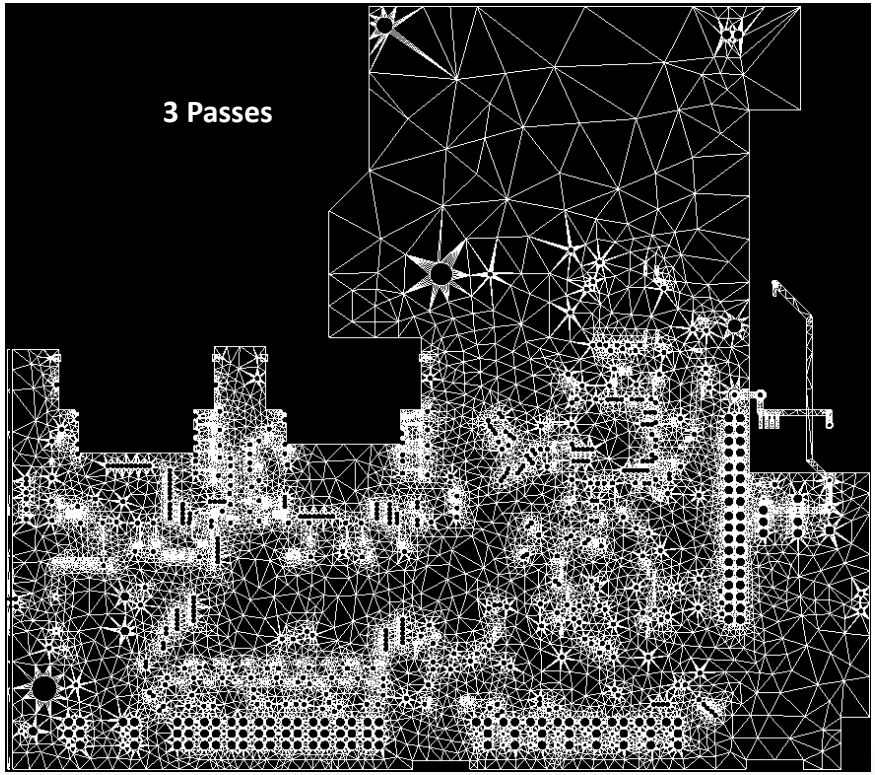
DC Adaptive Mesh Refinement

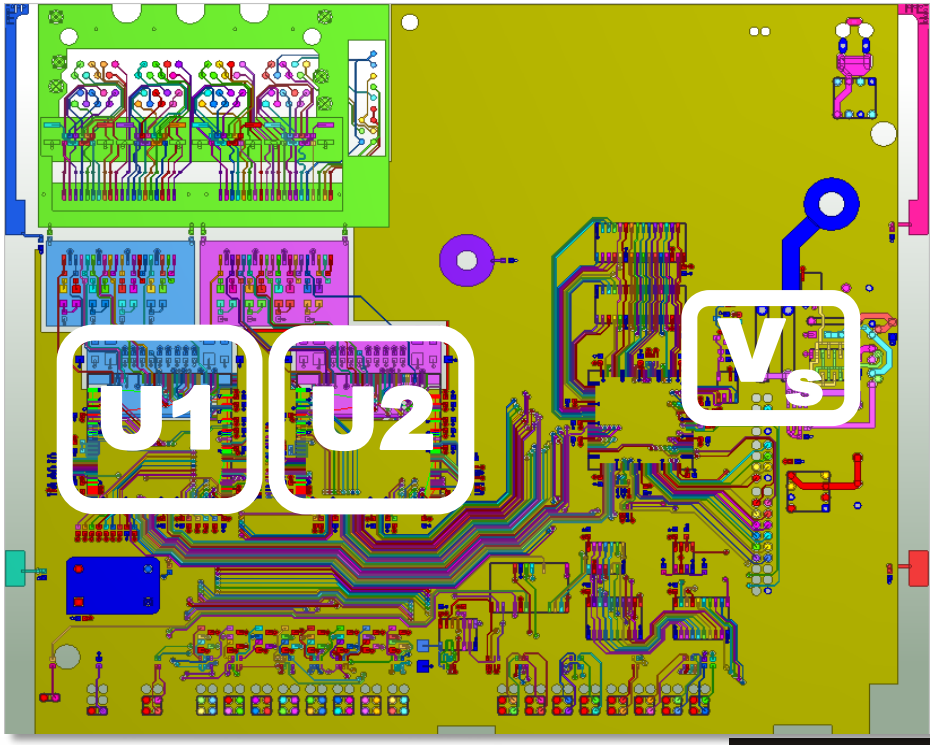
1 Adaptive Pass
3 Adaptive Passes
10 Adaptive Passes
20 Adaptive Passes



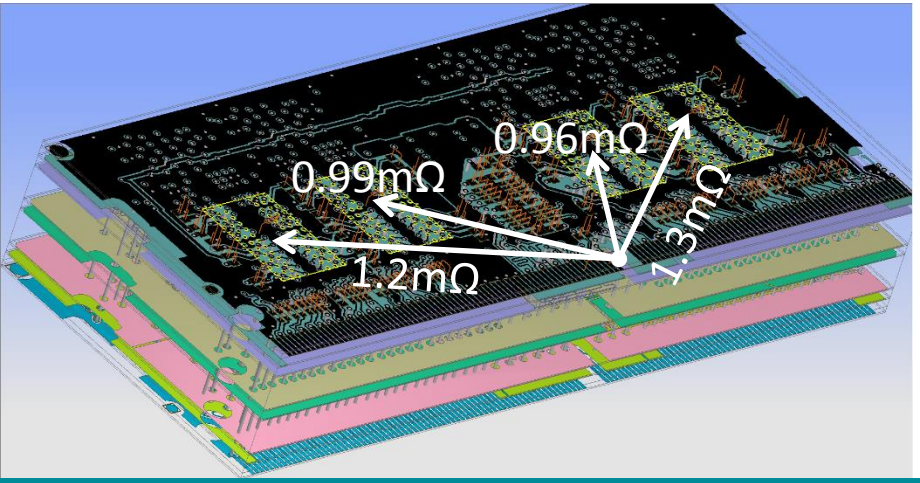
DC Results & Analysis

	Path Resistance Initial Mesh	Time & RAM	Path Resistance Adaptive Passes	Time & RAM
Voltage Source to U1 (path)	17.236 mΩ 1 - Pass	11 Seconds 6.7 MB	18.278 mΩ 3 – Adaptive Passes	17 Seconds 8.1 MB
Voltage Source to U2 (path)	16.850 mΩ 1 - Pass	10 Seconds 6.7 MB	17.870 mΩ 3 – Adaptive Passes	16 Seconds 8.1 MB

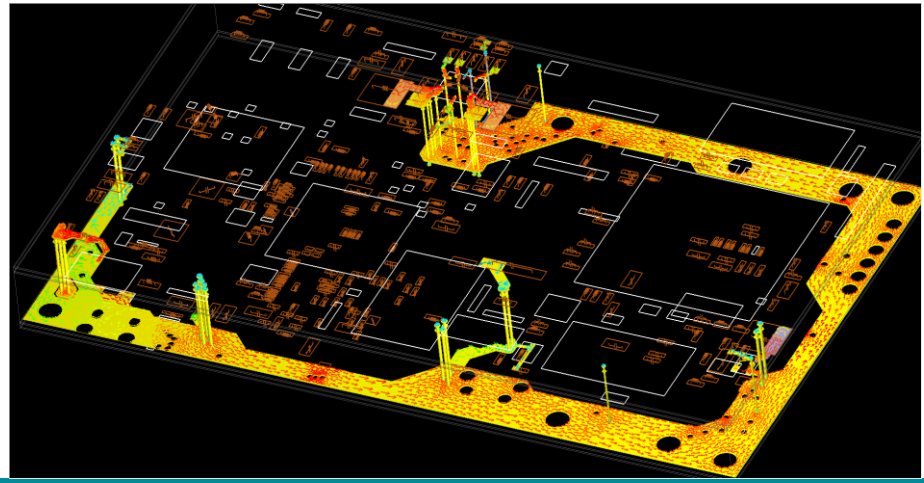




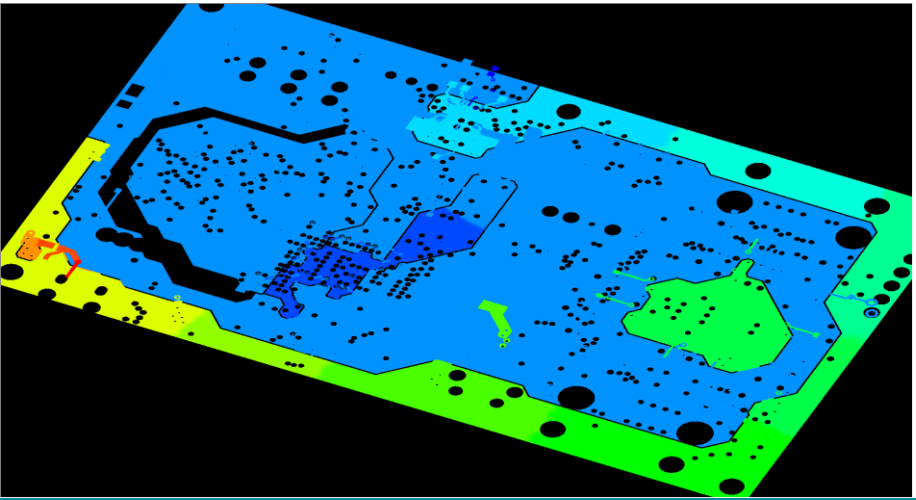
DC Results & Analysis



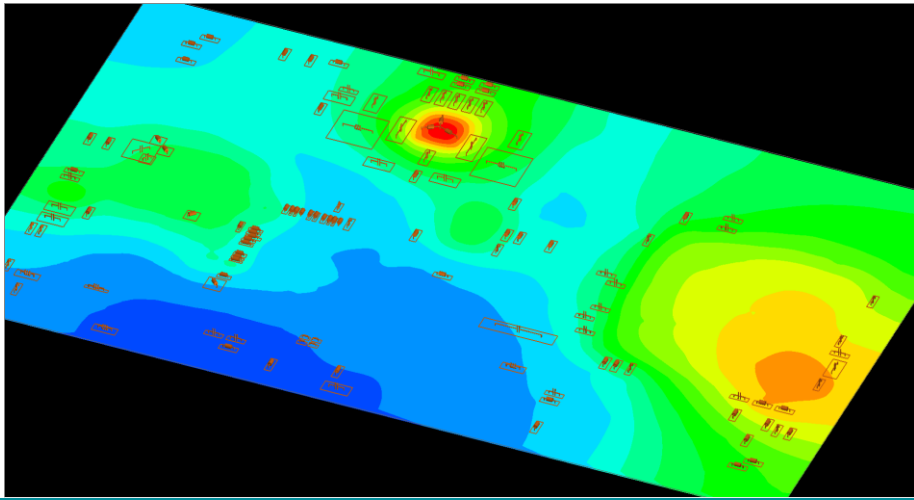
DC Path Resistance



Current Vectors Showing Electron Direction



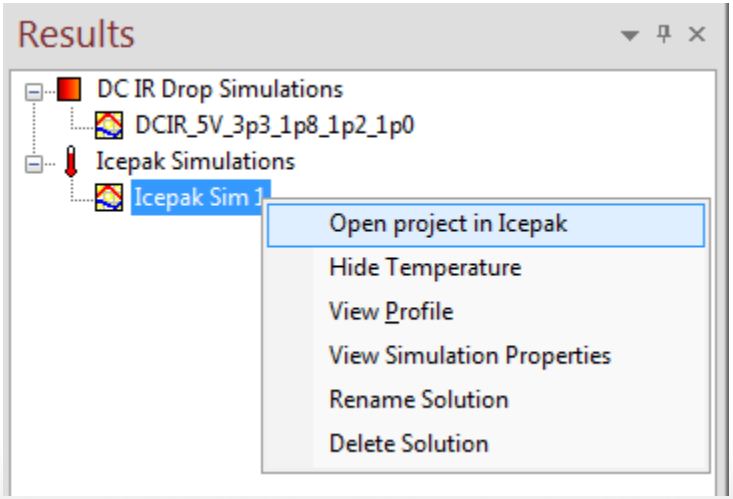
Power & Ground Plane Voltage Drop

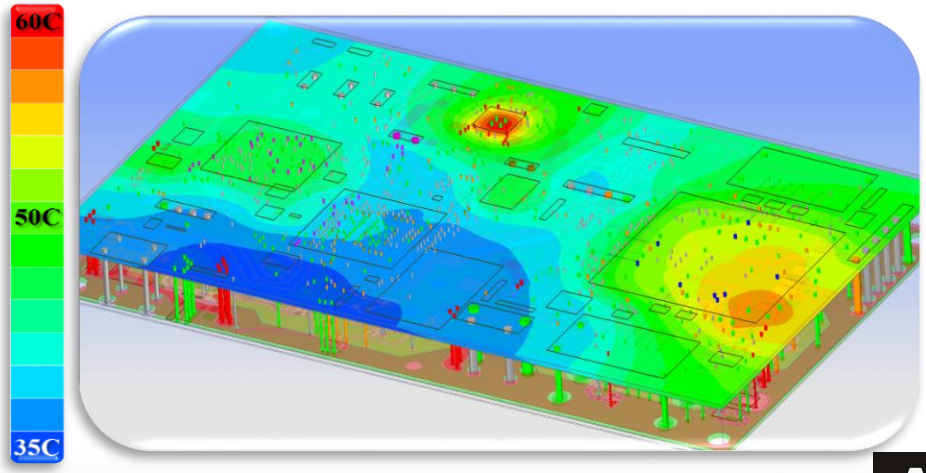


SIwave Thermal Solves using Icepak

SIwave Thermal Solutions using Icepak Solver

- **Joule Heating & Temperature analysis from SIwave**
  - **Uses Icepak Solver:**
    - **Joule Heating**
    - **Conduction only analysis**
    - **Forced convection (fan) analysis**
      - **Air can flow across (parallel) PCB or normal (perpendicular) to PCB**
    - **Natural convection analysis**
    - **Simplified cabinet enclosures included**
    - **Component power (Watts) allocation during setup**
  - **Ability to "Open" and perform more detailed analysis in Icepak GUI**





SIwave-PI

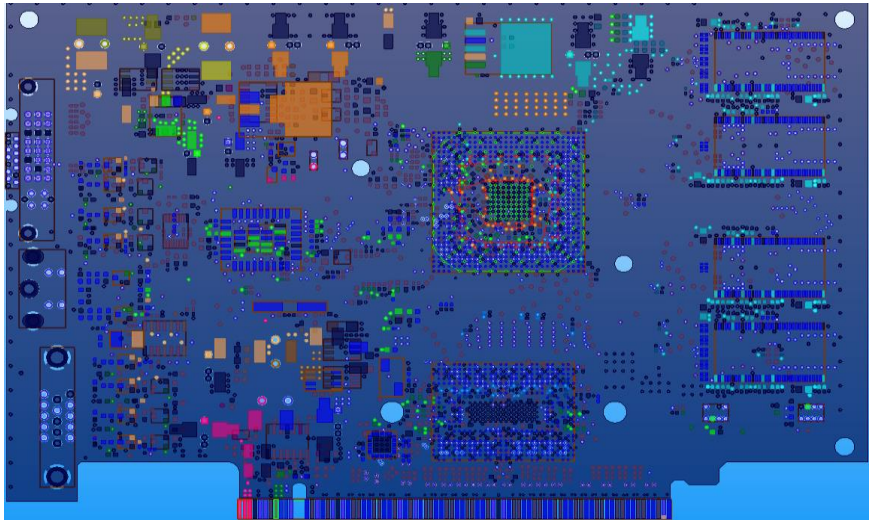
What is SIwave-PI?

- Power Integrity Platform utilized to Launch & Solve ECAD Simulations
- 2.5D & 3D Field Solvers
  - SIwave Hybrid AC & DC Solvers for PI
  - 3D Field Solvers for PI*
    - HFSS, Q3D Extractor, & PSI
- Models layered structures (Chip, PKG, & PCB)
- Creates 3D MCAD models for ANSYS Workbench, Q3D Extractor & HFSS

Analyses performed by SIwave-PI Core Solvers

- Power Integrity
  - 3D DC Resistance Solver with Adaptive Mesh Refinement
  - 2.5D Resonance Solver
  - 2.5D Driven Terminal Frequency Sweep Solver
  - 2.5D AC SYZ Solver
  - 2.5D Capacitor Loop Inductance Solver
  - PDN Channel Builder: Creates Apache RedHawk Model
  - PI Advisor: 2.5D AC SYZ Decoupling Capacitor Optimizer

PCIe Card Power Distribution



Analyses performed by SIwave-PI 3D Solvers*

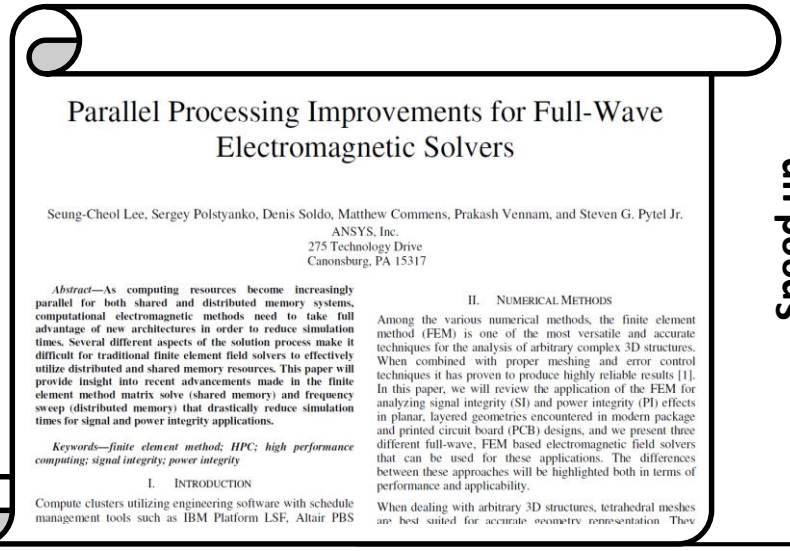
- Power Integrity
  - HFSS 3D Layout: General Purpose 3D Solver for PKG PI
  - PSI: 3D Prism Element Solver for Package PI
  - PI Advisor: Option to use PSI 3D Solver for Decoupling Capacitor Optimization
  - Q3D Extractor: Quasi-static Lumped RLC Extraction for PKG & PCBs
  - CPA: Full-wave RLC parasitic Extraction for PKGs

*Additional licenses required other than SIwave-PI

SIwave HPC Acceleration

Distributed Discrete S-Parameter Sweeps

– Shared and distributed memory operation



Parallel Processing Improvements for Full-Wave Electromagnetic Solvers

Seung-Cheol Lee, Sergey Polstyanko, Denis Soldo, Matthew Commens, Prakash Vennam, and Steven G. Pytel Jr.
ANSYS, Inc.
275 Technology Drive
Canonsburg, PA 15317

Abstract—As computing resources become increasingly parallel for both shared and distributed memory systems, computational electromagnetic methods need to take full advantage of new architectures in order to reduce simulation times. Several different aspects of the solution process make it difficult for traditional finite element field solvers to effectively utilize distributed and shared memory resources. This paper will provide insight into recent advancements made in the finite element method matrix solve (shared memory) and frequency sweep (distributed memory) that drastically reduce simulation times for signal and power integrity applications.

Keywords—finite element method; HPC; high performance computing; signal integrity; power integrity

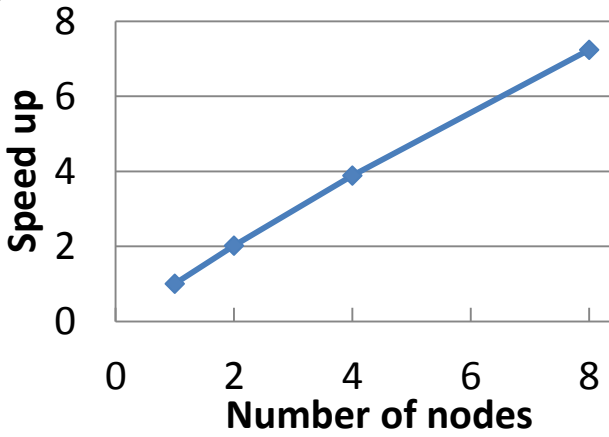
I. Introduction

Compute clusters utilizing engineering software with schedule management tools such as IBM Platform LSF, Altair PBS

II. Numerical Methods

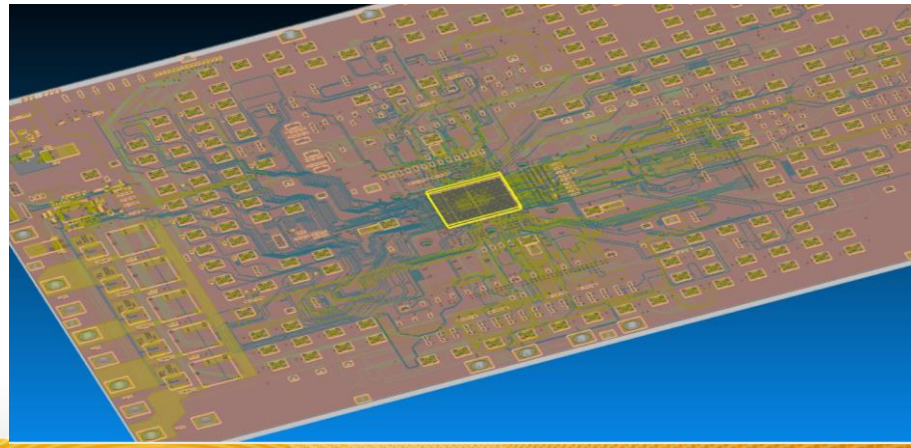
Among the various numerical methods, the finite element method (FEM) is one of the most versatile and accurate techniques for the analysis of arbitrary complex 3D structures. When combined with proper meshing and error control techniques it has proven to produce highly reliable results [1]. In this paper, we will review the application of the FEM for analyzing signal integrity (SI) and power integrity (PI) effects in planar, layered geometries encountered in modern package and printed circuit board (PCB) designs, and we present three different full-wave, FEM based electromagnetic field solvers that can be used for these applications. The differences between these approaches will be highlighted both in terms of performance and applicability.

When dealing with arbitrary 3D structures, tetrahedral meshes are best suited for accurate geometry representation. They



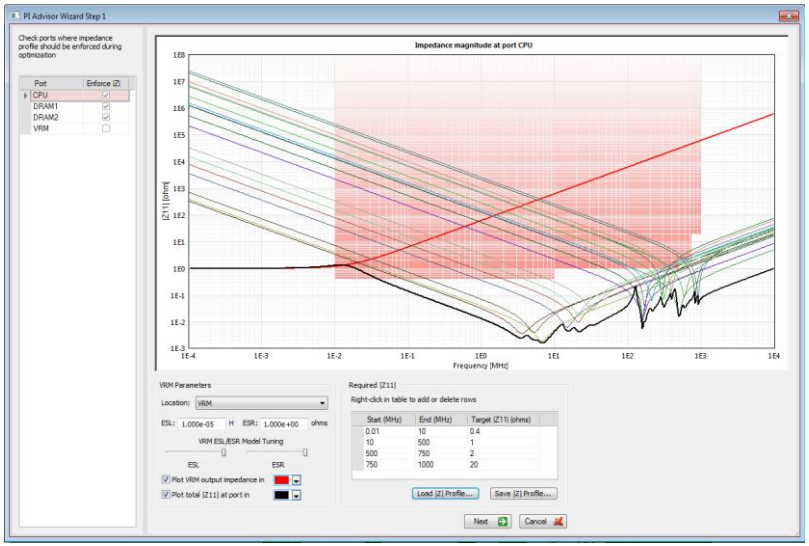
scalability > 90%

Cores	Configuration	Runtime	Speed Up
1	1 node	92hr 39 min	1x
16	1 node	16hr 18min	6x
32	2 nodes	5hr 28min	17x
64	4 nodes,	2hr 50min	33x
128	8 nodes	1hr 31min	**61x**



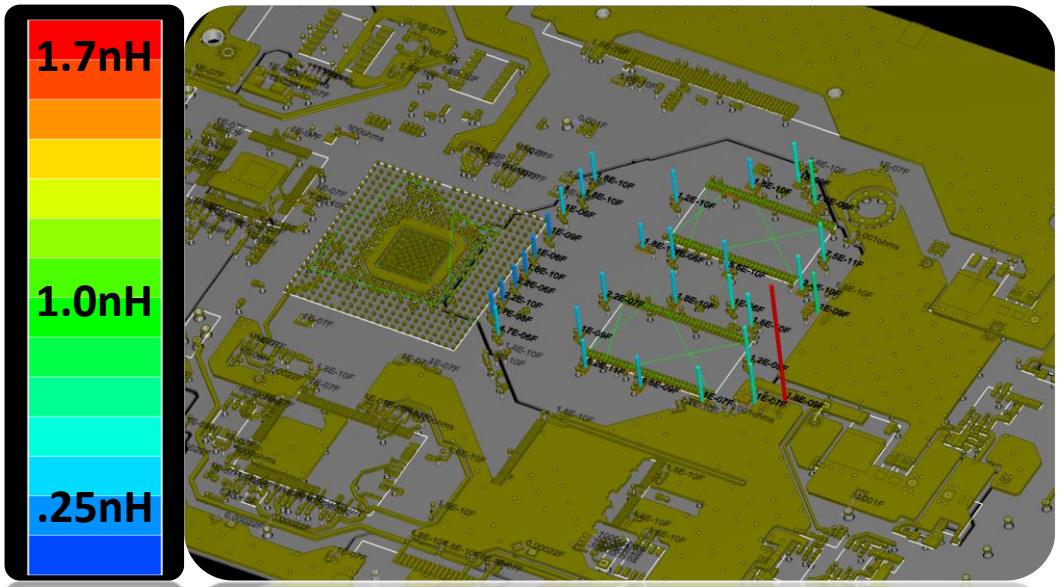
PI Advisor: Automated PI Analysis

Optimizes Decoupling Capacitors for Power Integrity



- SIwave AC Solver or PSI AC Solver

- SIwave AC Solve Time = 15 min 7 sec
  - Frequency Setup
    - 1KHz <= f < 1GHz
  - Genetic Algorithm Setup
    - Optimized for Impedance
    - Optimized for Total Number of Caps
    - Optimized for Capacitor Types
    - Optimized for Price
- Original solution
  - Total # Caps: 74
- Optimized Solution
  - Total # Caps: 18
  - Capacitor Types = 5
    - AVX, Samsung, and Kemet



SIwave

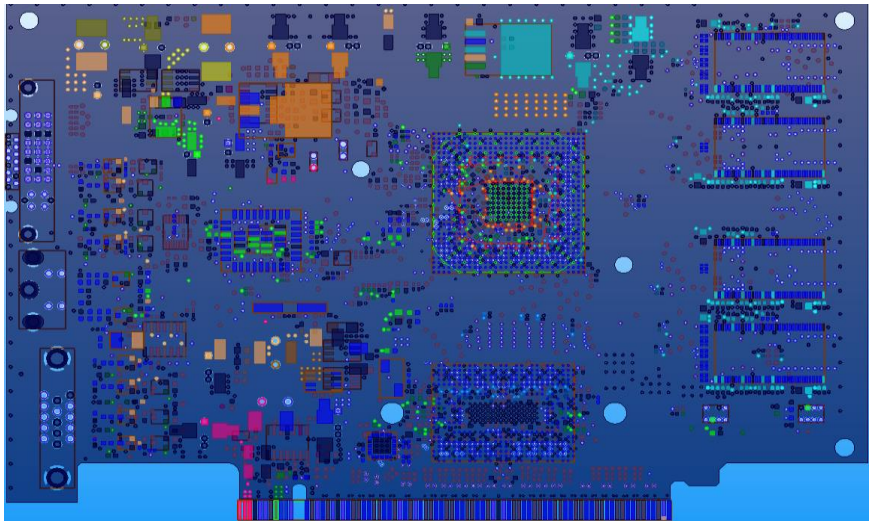
What is SIwave?

- Platform to Launch & Solve ECAD Simulations
- Field Solvers
  - HFSS, Q3D Extractor, CPA, & PSI
- Thermal Solves
  - Icepak
- Circuit Solvers
  - Nexxim & Synopsys HSPICE
- Models layered structures (PKG & PCB)
- Creates 3D MCAD models for ANSYS Workbench, Q3D Extractor & HFSS

Analyses performed by SIwave Core Solvers

- Power Integrity
  - 3D DCR Solver with Adaptive Mesh Refinement
  - 2.5D Resonance Solver
  - 2.5D Driven Terminal Frequency Sweep Solver
  - 2.5D AC SYZ Solver
  - 2.5D Capacitor Loop Inductance Solver
  - PDN Channel Builder: Creates Apache RedHawk Model
  - PI Advisor: 2.5D AC SYZ Decoupling Capacitor Optimizer

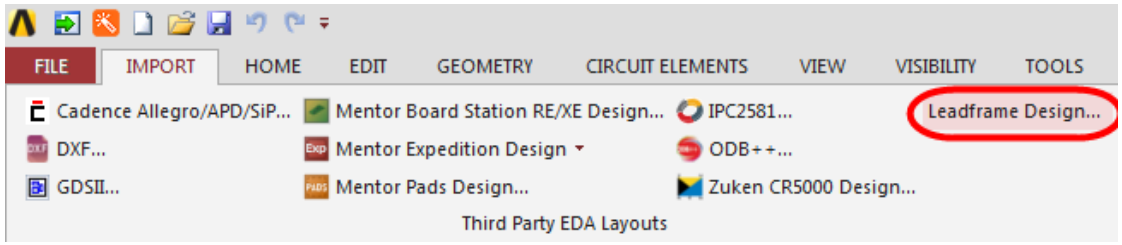
PCIe Card Power Distribution

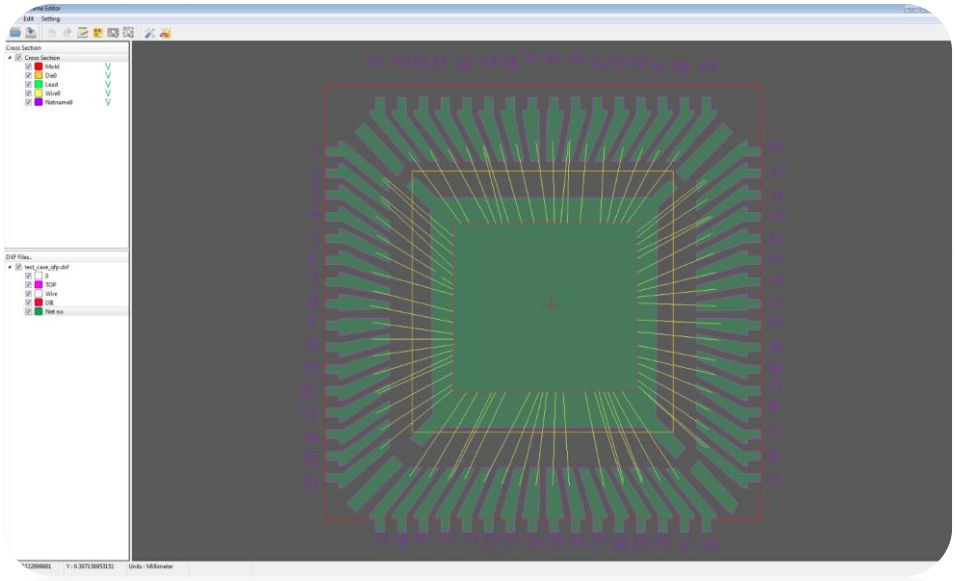


Analyses performed by SIwave Core Solvers

- Signal Integrity
  - Zo & Crosstalk scans for PCB & PKGs
  - 2.5D AC SYZ solver: Fast, High Capacity Hybrid Solver
  - Signal Net Analyzer: Impedance & Flight Time Solves
  - SIwizard: Creates & Solves Transient CKT Schematics
  - TDR wizard
- EMI/EMC
  - 2.5D Near-Field Solver
  - 2.5D Far-Field Solver
  - 2.5D Driven Terminal Frequency Sweep Solver
  - 2.5D Resonance Solver

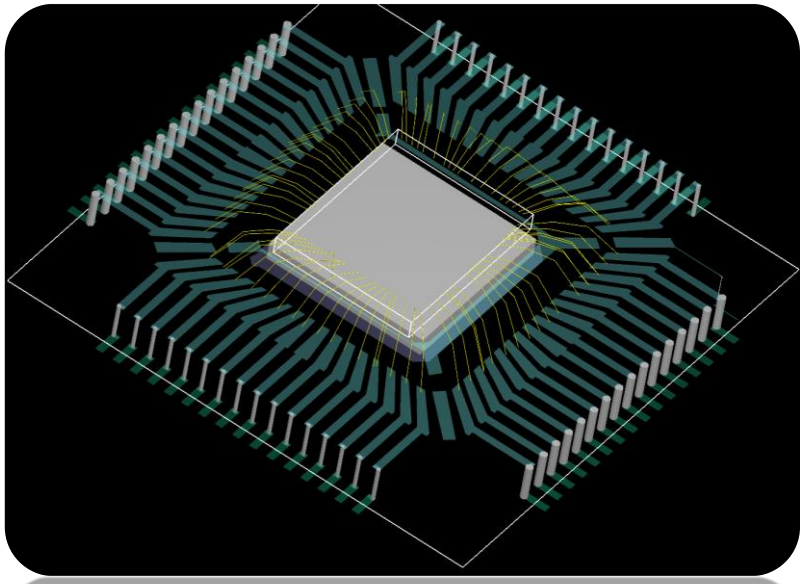
Leadframe Editor





Lead Frame Editor

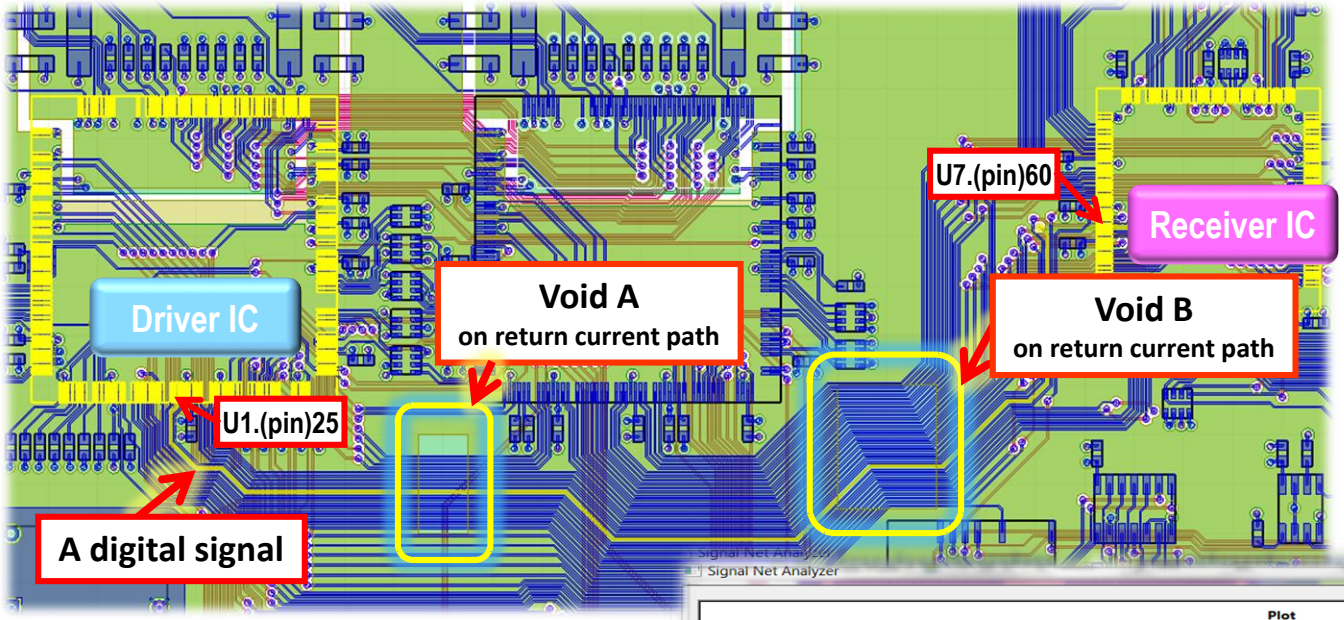
- Creates SIwave & 3D Layout .anf Geometries
- Creates HFSS & Q3D .sat Geometries



Lead Frame Editor

- SIwave QFP Package from Lead Frame Editor

Impedance & Flight Time Calculations

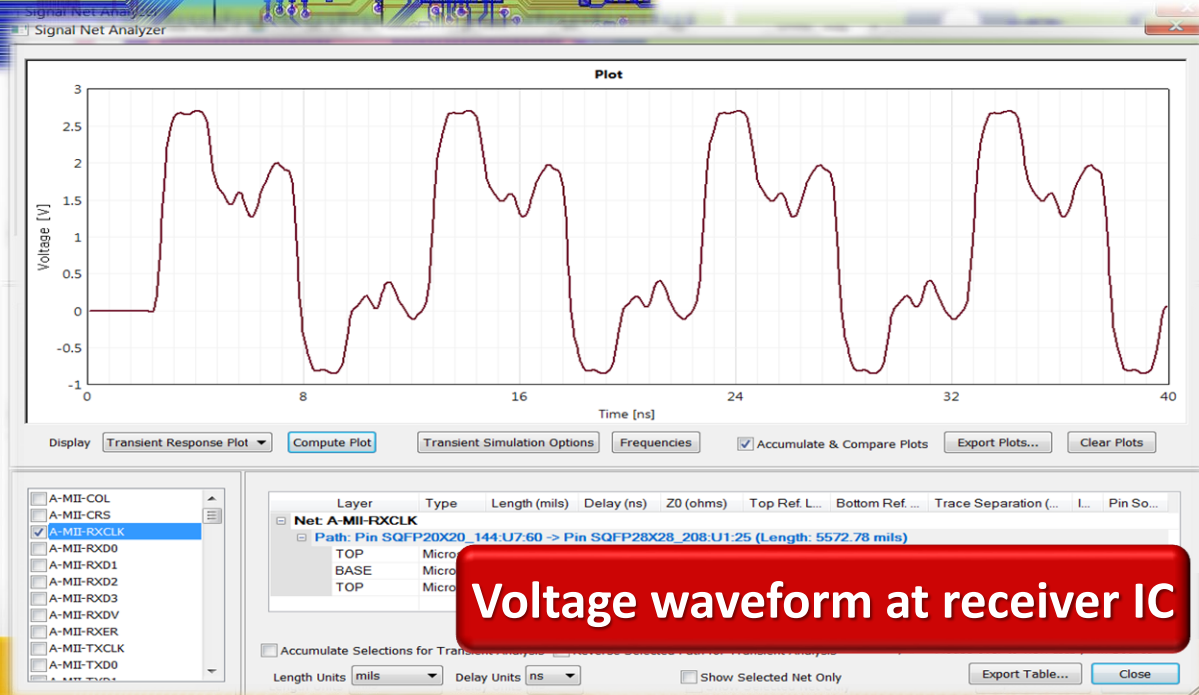


Signal Net Analyzer

SNA provides:

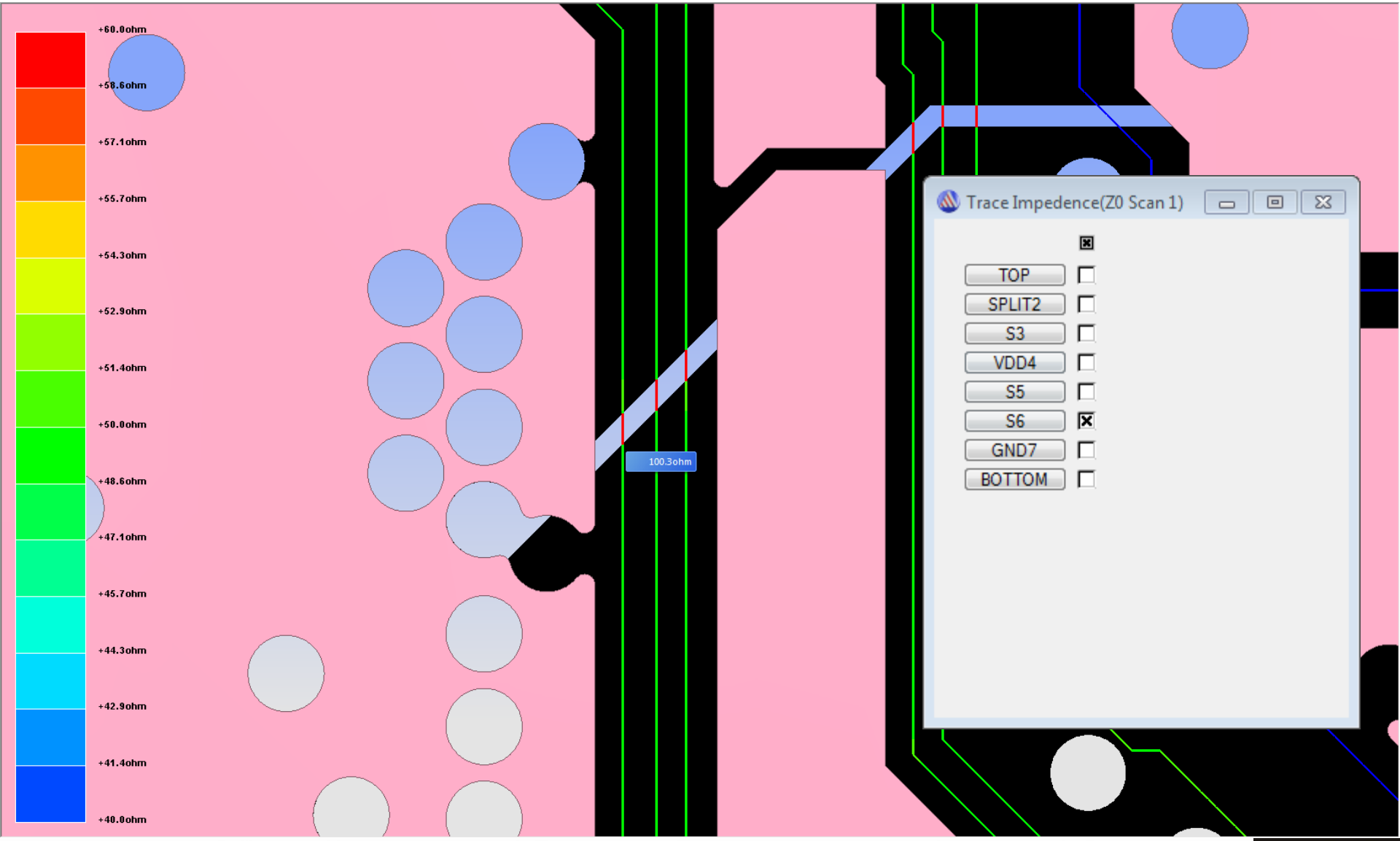
1. Z_o Profile & Delay for all paths of a signal.

2. Reflection Noise through transient analysis.

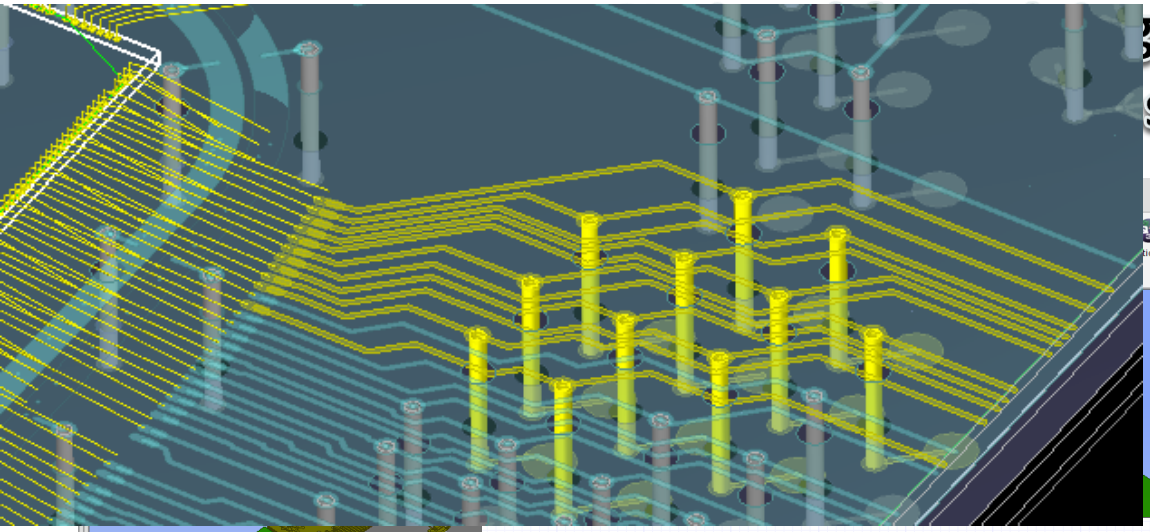


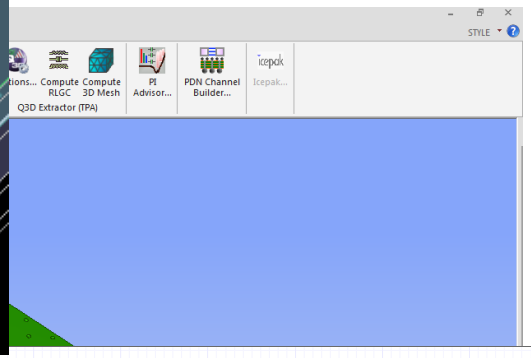
Voltage waveform at receiver IC

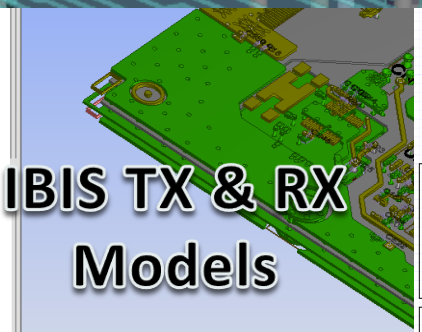
Zo Scans (SE & Differential) with Reporting



Create & Solve Circuit Schematics

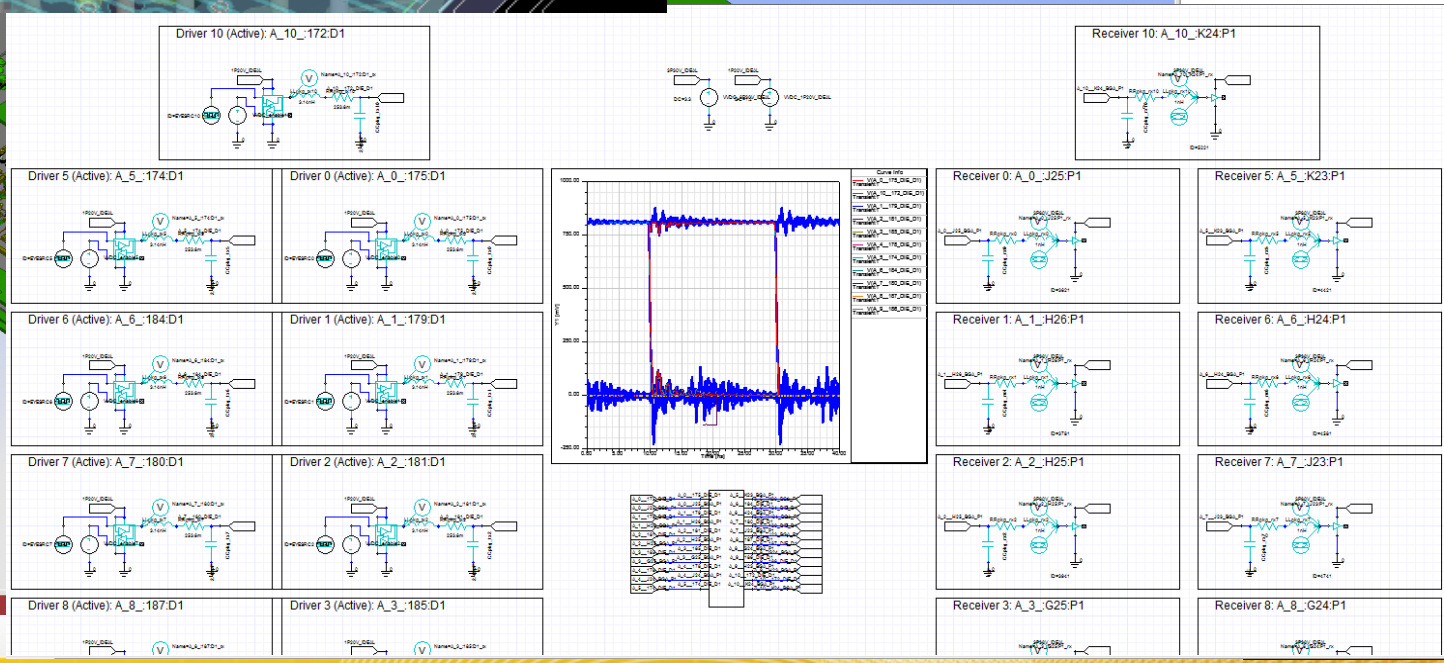






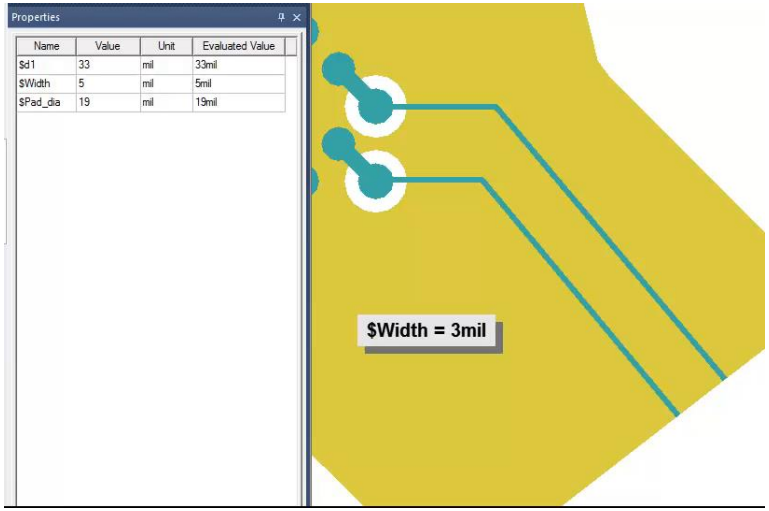
IBIS TX & RX Models

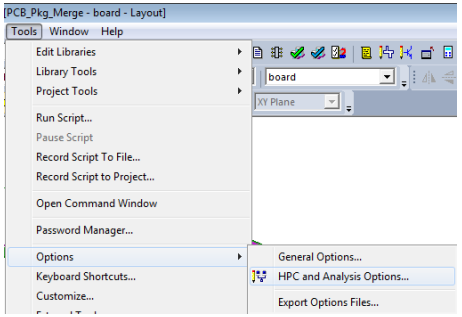
Circuit Analysis
- Transient
- QuickEye

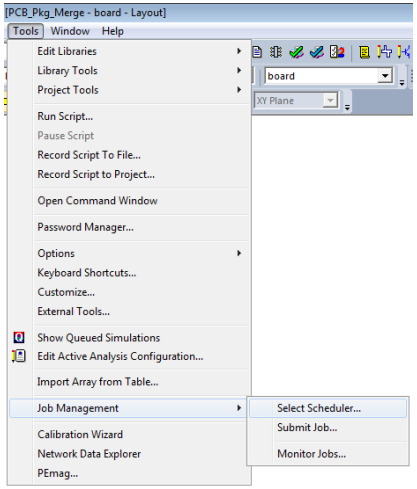


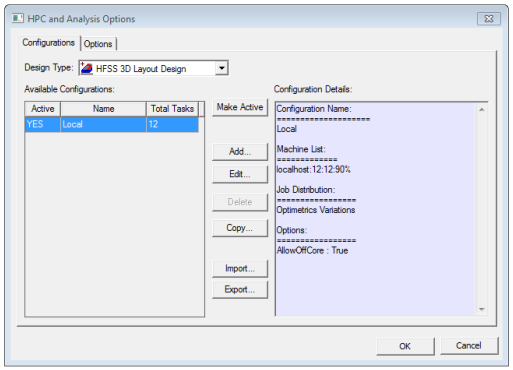
SIwave SYZ Solver Integration into AEDT 3D Layout

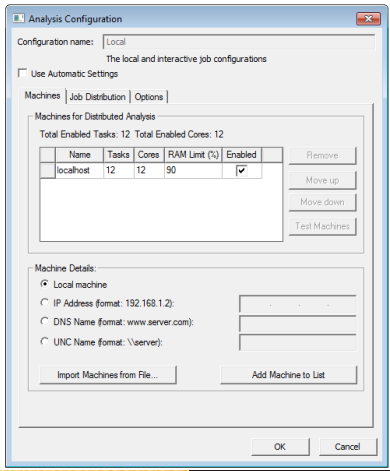
- SIwave Solution Setups are now part of ANSYS Electronics Desktop 3D Layout
- Enables parametric solves
- Enables usage of Electromagnetics RSM



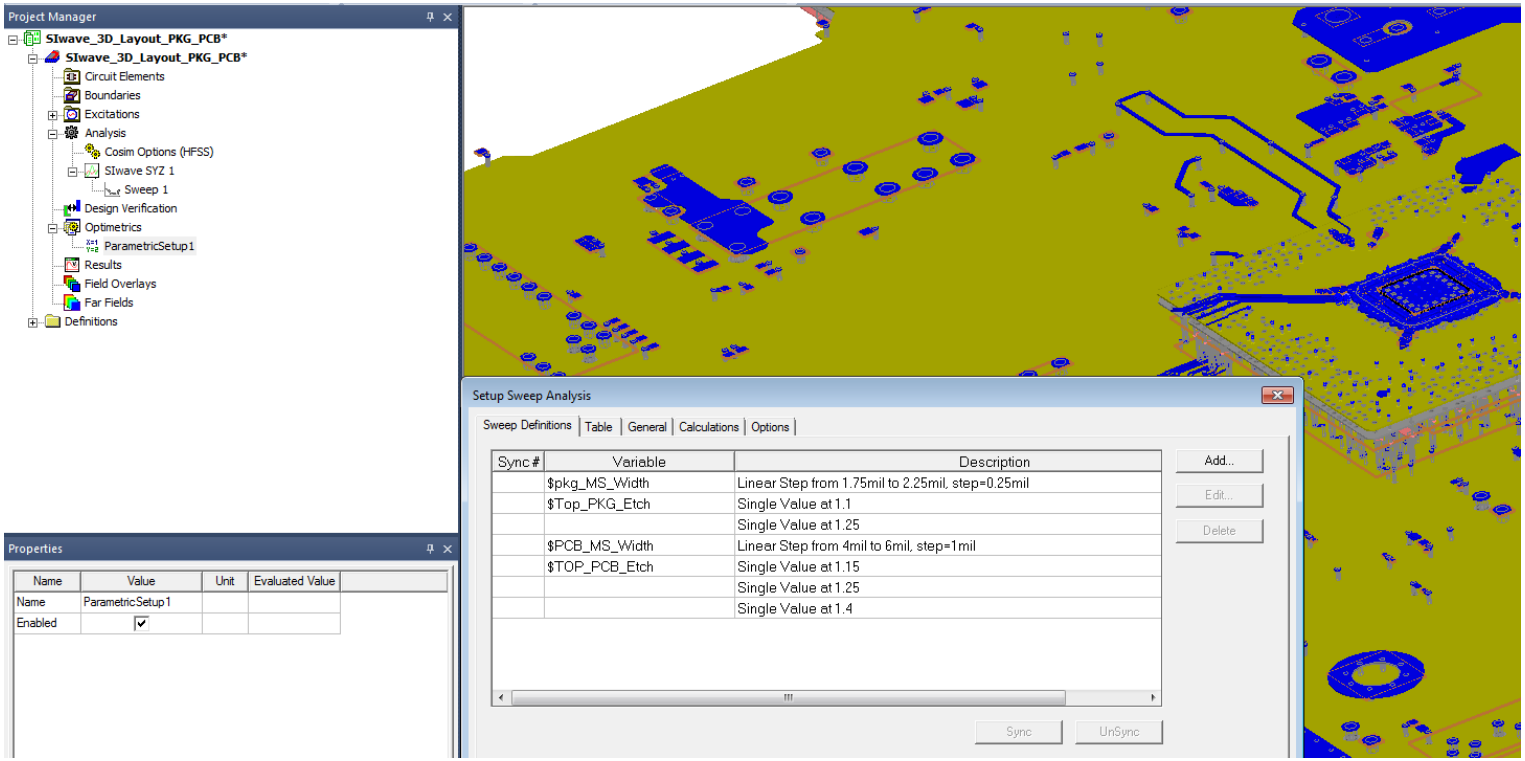


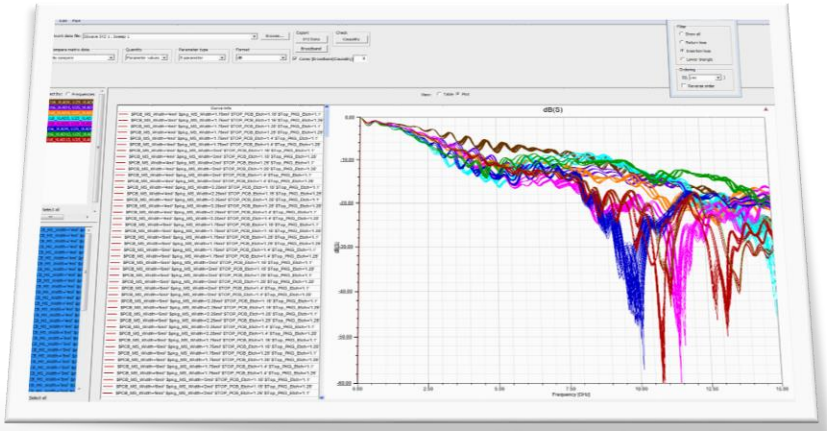


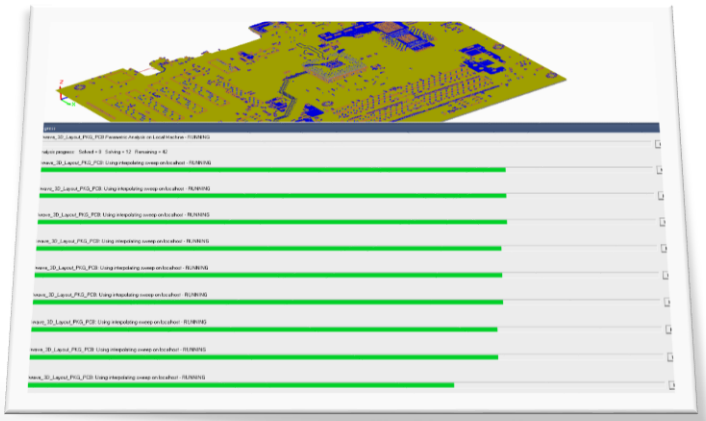




SIwave Parametric Design within AEDT 3D Layout

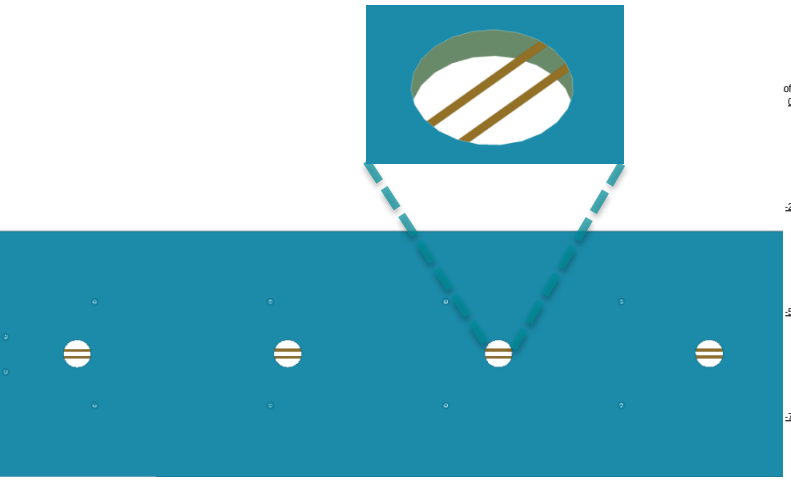




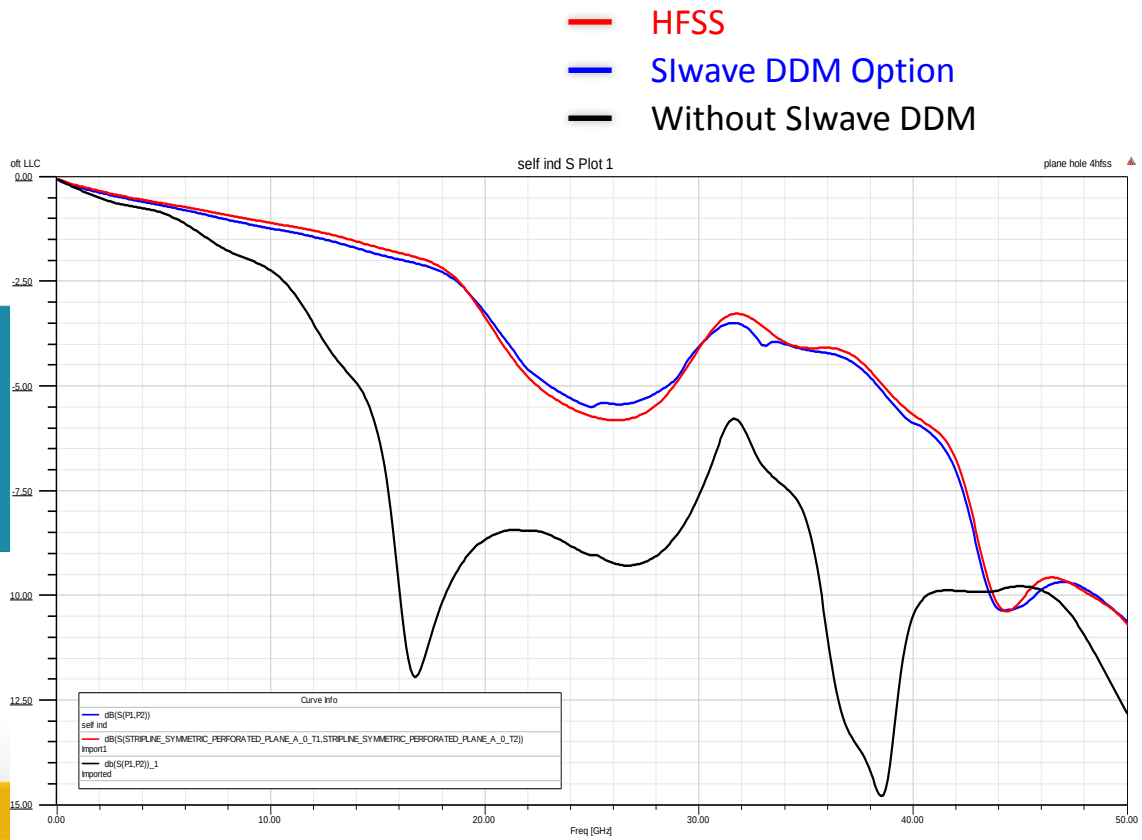


Improved AC SYZ Accuracy

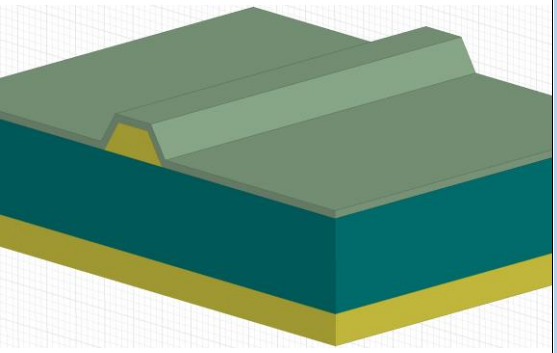
- **Advanced 3D DDM solver improves accuracy for**
  - **Traces routed across splits, unreferenced traces, poorly referenced ports, vias & large antipads**

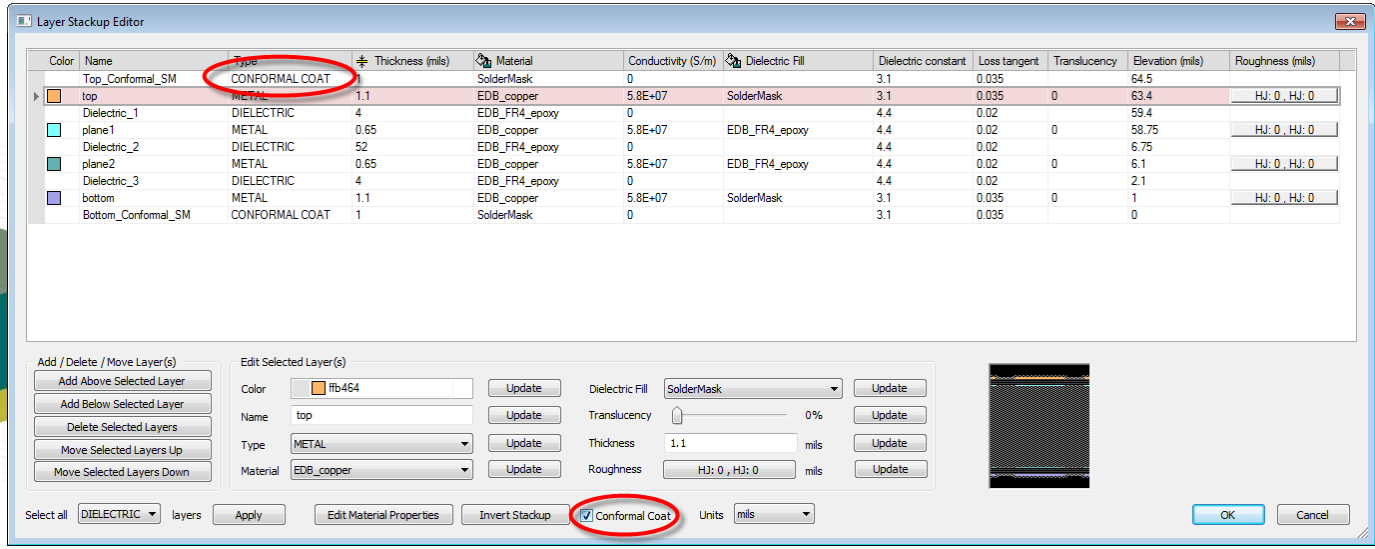


Unreferenced Traces

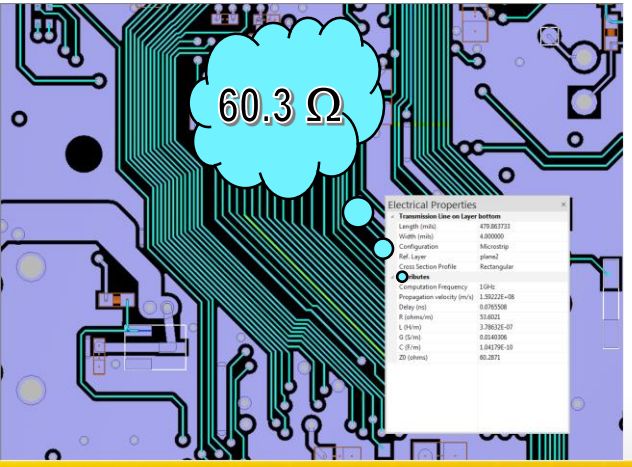


SIwave Conformal Soldermasks

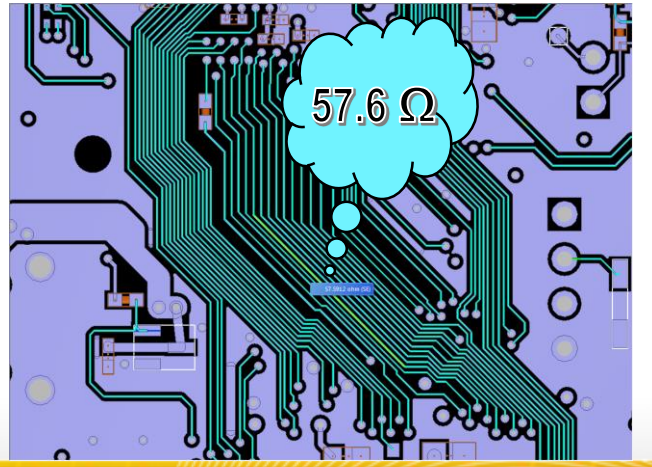




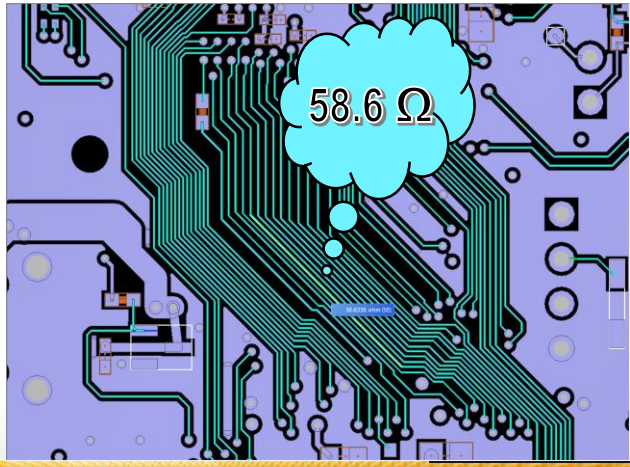
Single Ended Zo
Without Trace-Trace Coupling
Without Conformal Soldermask



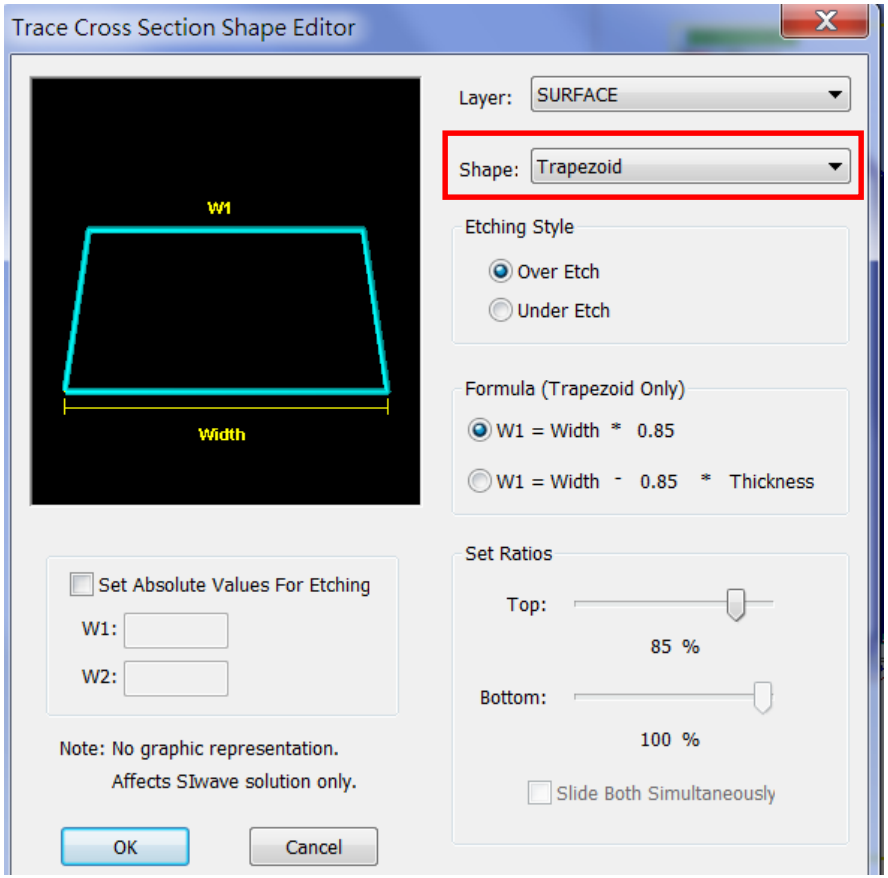
Single Ended Zo
With Trace-Trace Coupling
Without Conformal Soldermask

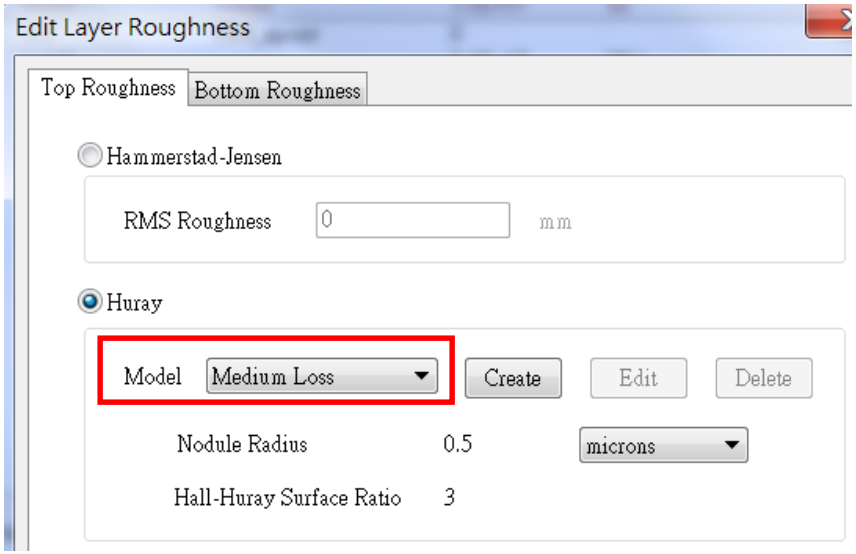


Single Ended Zo
With Trace-Trace Coupling
With Conformal Soldermask



Trace Cross Section and Surface Roughness

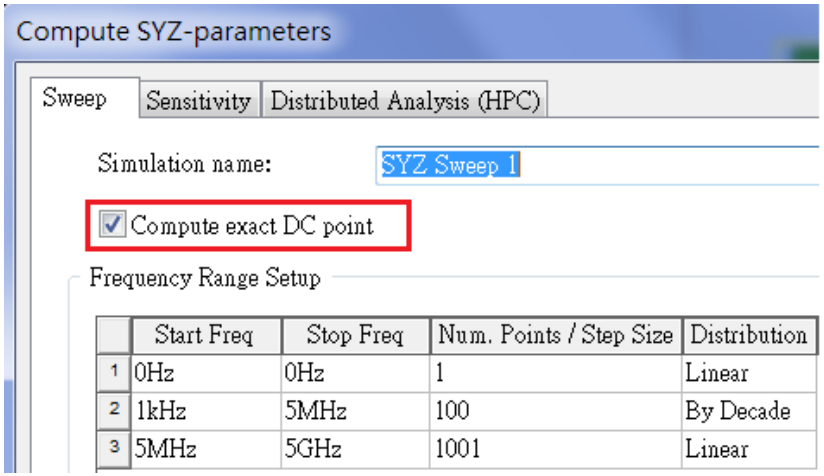




Combined AC and DC simulation results

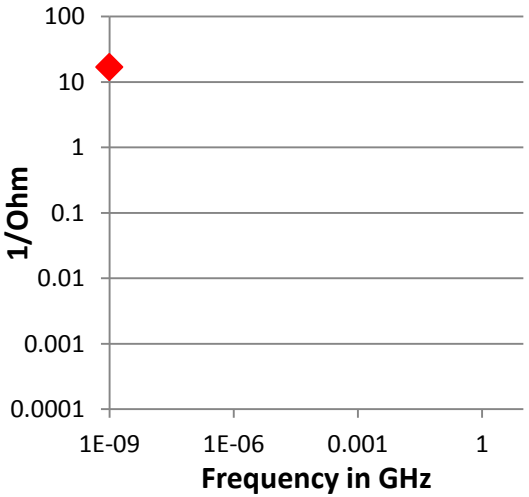
Merging DCR point with frequency-swept AC results

Improved accuracy over the entire frequency bandwidth

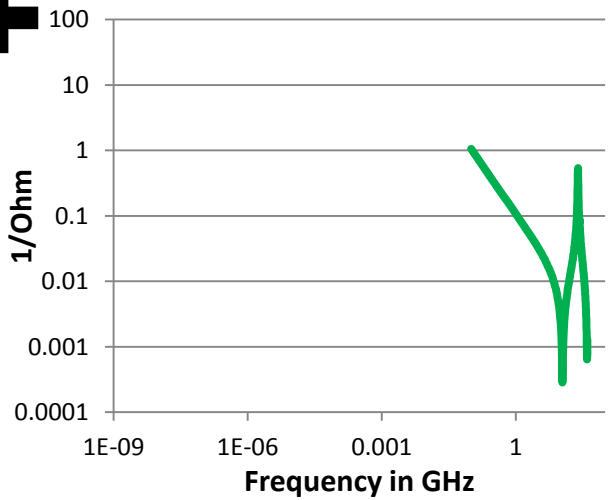


	Start Freq	Stop Freq	Num. Points / Step Size	Distribution
1	0Hz	0Hz	1	Linear
2	1kHz	5MHz	100	By Decade
3	5MHz	5GHz	1001	Linear

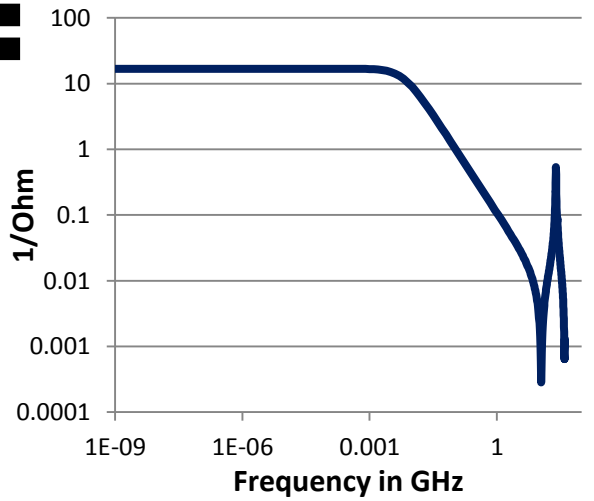
DCIR



SYZ



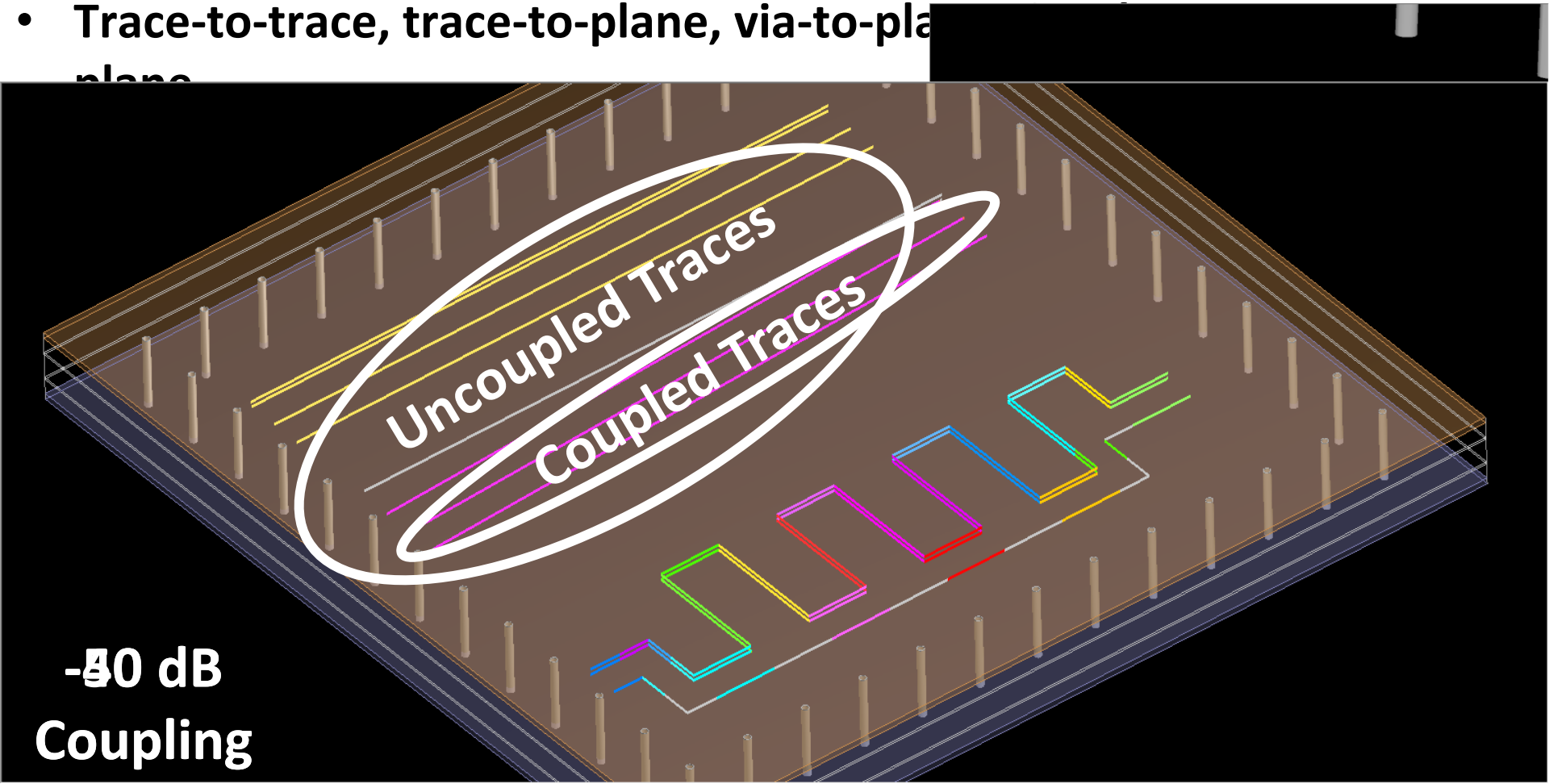
DCIR + SYZ



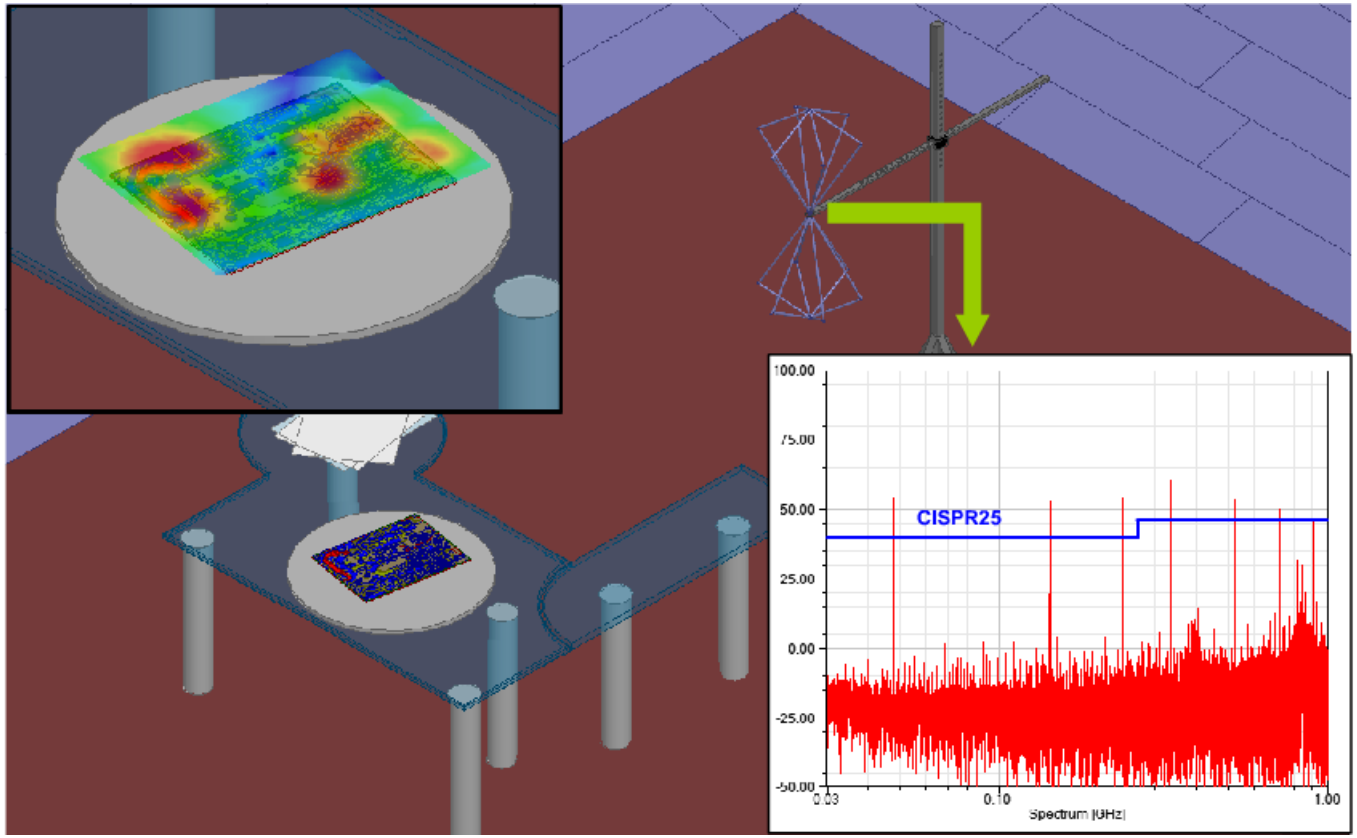
Coupling

- Color indicates coupled segments (not magnitude)
- Broadside coupled traces are included

- **All models coupled together when appropriate**
- **Trace-to-trace, trace-to-plane, via-to-pla**
  plane



SIwave & HFSS EMI Virtual Compliance



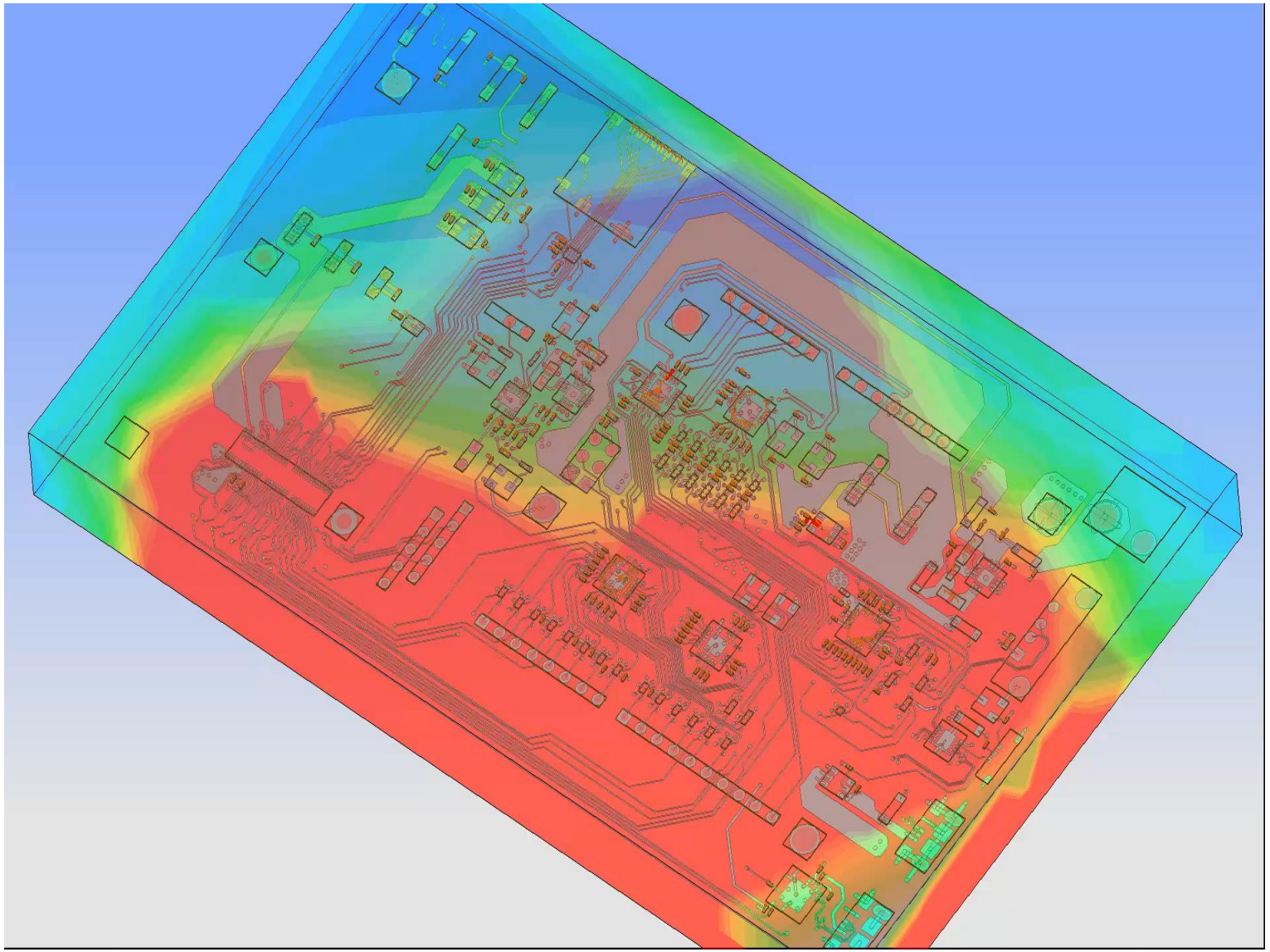
RADIATED EMISSIONS

This example shows radiated emissions (using a Quasi Peak detector) that are captured by the bi-conical antenna for every angular position of the PCB simulated in SIwave.

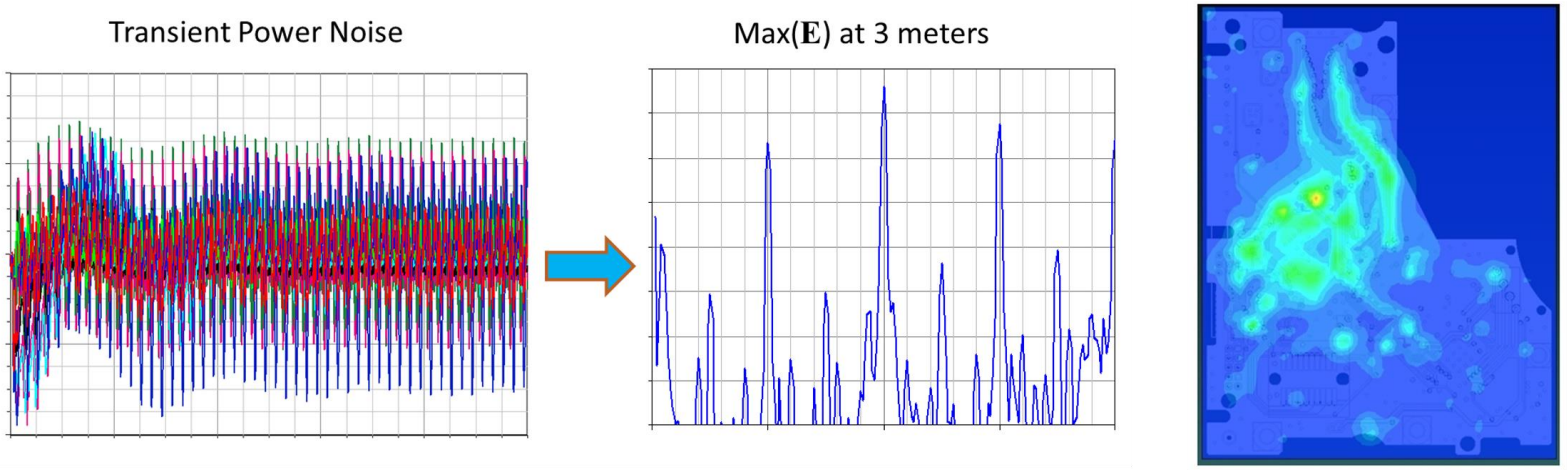
PCB MODEL COURTESY OF INOVAX

ANSYS

SIwave Near-Field EMI

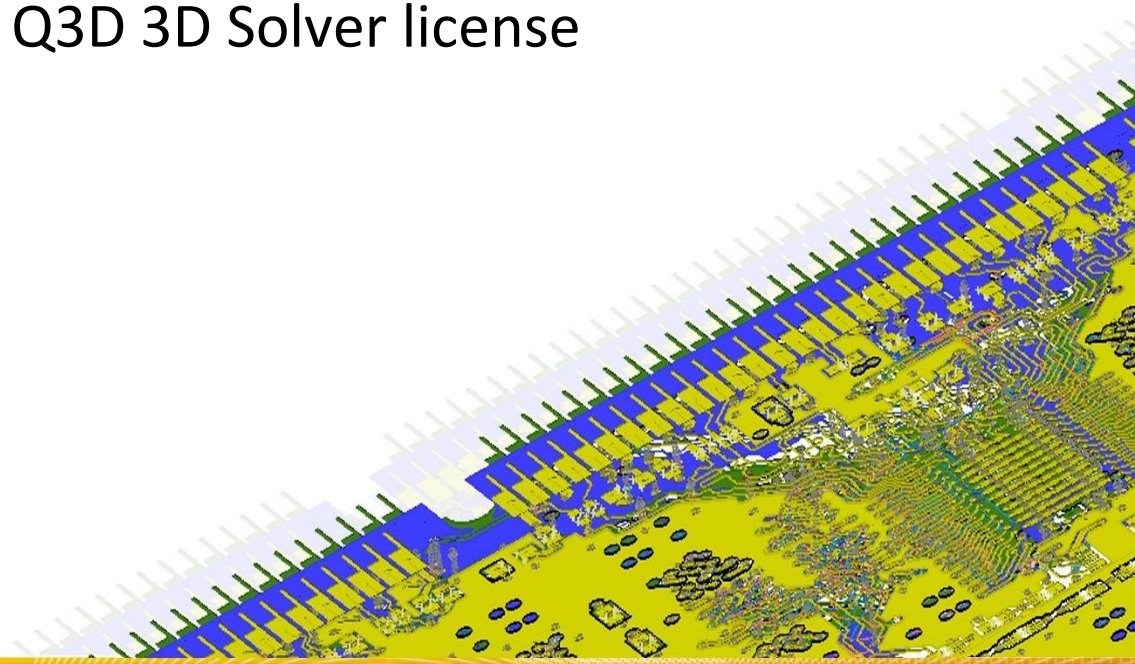


Conducted EMI with CPM



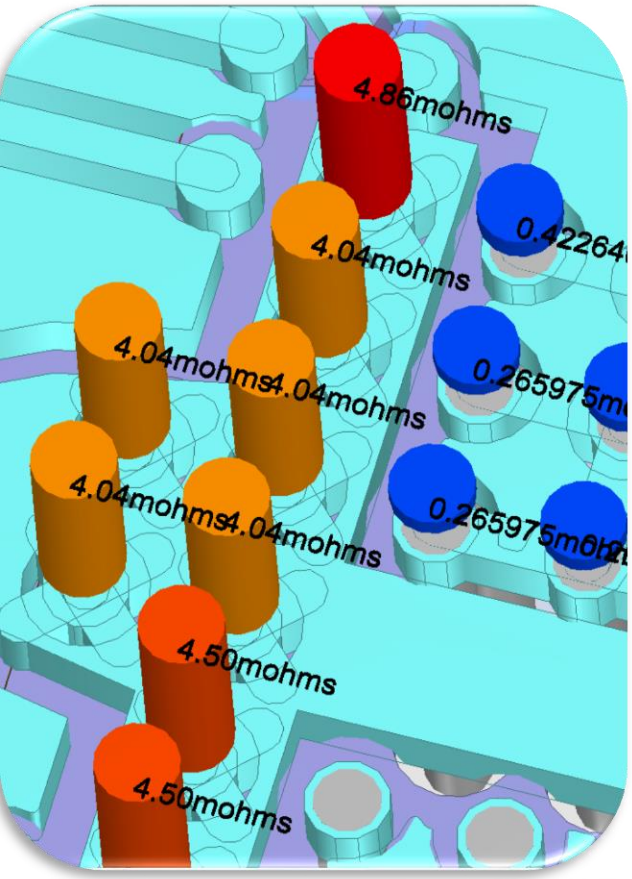
SIwave-CPA

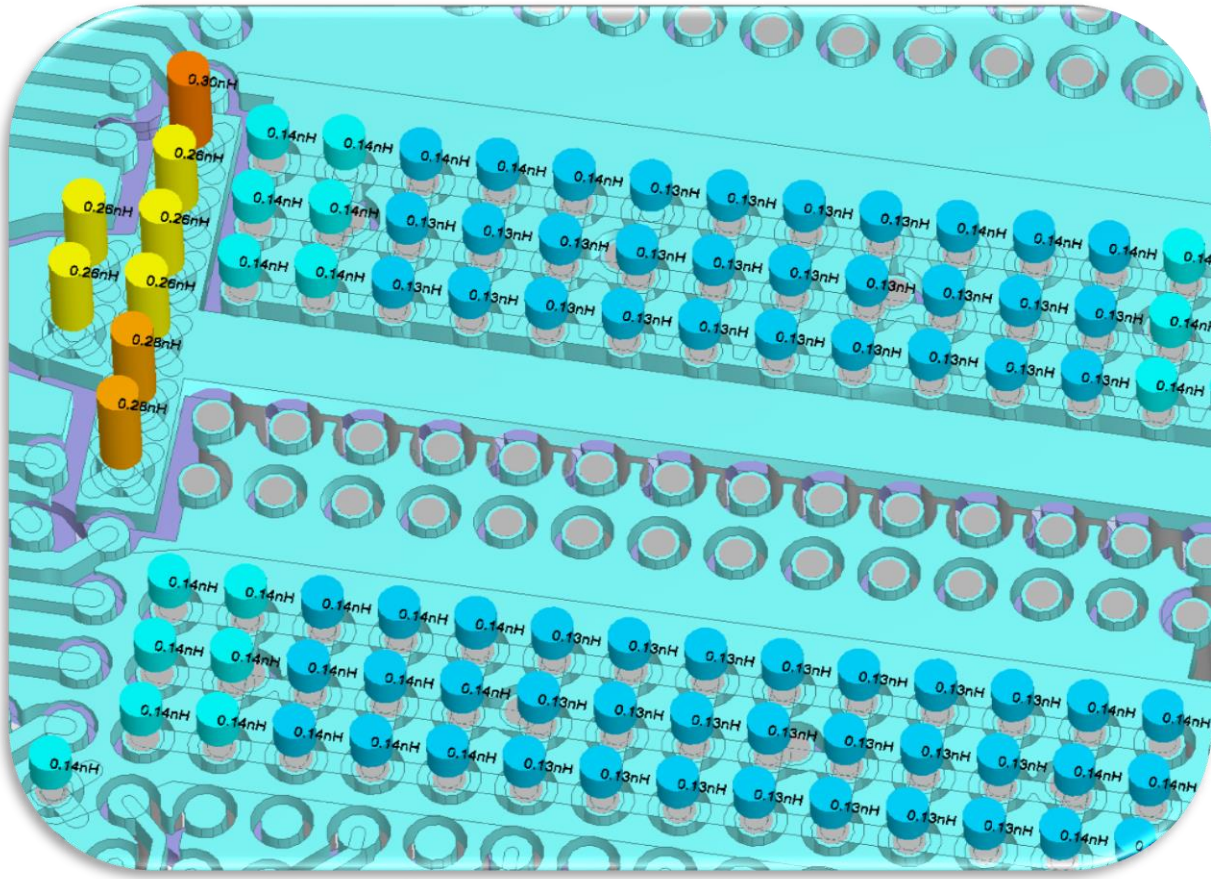
Requires Q3D 3D Solver license



What is SIwave-CPA?

- **The CPA (Chip-Package-Analysis) solver is a 3D full-wave, FEM based solver for fast and accurate extraction of RLC parasitics.**
  - **It is optimized to analyze power and signal nets on packages**





SIwave-CPA

- Automated .html reporting for partial and loop resistance/inductance
- The CPA solver is capable of producing per bump/ball resolution RLC extracted parasitics
- Visual Bar graph plotting is available for solderball/bump and Pin Groups

Flip-Chip PDN System

Solver	Net	R (mΩ)	L (nH)	C (pF)	Solve Time (minutes)	Speed Up	RAM (MB)	RAM Reduction
Q3D (TPA)	PDN A	12.3	310.6	24.8	4.51	-	748	-
CPA	PDN A	12.9	312.4	25.8	0.4	**11x**	210	**4x**
Q3D (TPA)	PDN B	9.1	224.8	24.8	4.51	-	748	-
CPA	PDN B	9.2	230.7	25.9	0.4	**11x**	210	**4x**

SIwave-CPA

Wirebond Package PDN System

Solver	Net	R (mΩ)	L (pH)	C (pF)	Solve Time (Hours)	Speed Up	RAM (GB)	RAM Reduction
Q3D (TPA)	PDN C	1.58	79.2	128.4	48	-	71	-
CPA	PDN C	1.61	79.9	129.3	0.1	**480x**	13	**5x**
Q3D (TPA)	PDN D	0.16	12.6	973.4	48	-	71	-
CPA	PDN D	0.16	12.9	979.3	0.1	**480x**	13	**5x**

Coupled Microstrip Lines

Solver	Net	R (mΩ)	L (nH)	C (pF)	Solve Time (Minutes)	Speed Up	RAM (MB)	RAM Reduction
NPE	Trace A	386	3.42	1.17	3.0	-	450	-
CPA	Trace A	386	3.22	1.17	1.0	**3x**	300	**3x**
NPE	Trace B	386	3.44	1.19	3.0	-	450	-
CPA	Trace B	386	3.30	1.17	1.0	**3x**	300	**3x**